SOFTWARE DEFINED RADIO TEST BED FOR INTEGRATED COMMUNICATIONS AND NAVIGATION APPLICATIONS

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ABSTRACT

Accurate positioning is an essential element of next generation Software Defined Radio (SDR) applications such as cognitive radios, telematics, and E-9-1-1, leading to an increased demand for GPS waveforms on SDR platforms. The Software GPS Receiver (SGR) developed in-house at NAVSYS implements functionality largely in software, and uses a reprogrammable hardware platform that can also be configured to perform other communication functions. Further, the sensors compatible with this system can provide GPS, wireless, inertial, and image information for a diverse set of applications. The low cost PC/104-based SDR test bed developed at NAVSYS can input communication and GPS signals operating at different frequencies using up to eight Digital Antenna Elements (DAE). A PC/104 compatible Field Programmable Gate Array (FPGA) card is used to perform high-speed signal processing operations. This paper presents the design of the PC/104-based test bed that can be used for developing and testing GPS and other basic communication waveforms for SDR applications.

1. INTRODUCTION

As Software Defined Radios acquire intelligence and cognitive abilities, knowledge of the user's location becomes an integral aspect of the system functionality. Accurate knowledge of the user's location enables a cognitive radio to identify and tune information about services in the vicinity and provide appropriate guidance to the user. Additionally, telematics applications and E-9-1-1 services also require knowledge of the user's location. In order to realize these intelligent SDRs, it has become imperative to incorporate GPS waveforms into the SDR framework.

NAVSYS has developed a PC/104-based Software Defined Radio test bed that can be used for developing and testing integrated communication and navigation SDR applications [1].

The PC/104-Plus test bed is used to implement the hardware functionality of the Software GPS Receiver also developed at NAVSYS. The hardware test bed is used to input the RF signal, downconvert it to baseband and perform high speed correlations for bit extraction. In addition, the sensors compatible with this system can provide GPS, wireless, inertial, and image information which can be used for the development of sophisticated location systems. The compact form factor of the PC/104 enables the test bed to be portable which allows for convenient outdoor and indoor testing.

The test bed adopts a modular design based on low-cost hardware and software that can be configured to input communication and GPS signals operating at different frequencies. The digitized GPS or communication signals are generated using multiple simplified RF front-end devices called Digital Antenna Elements, also developed at NAVSYS. These sub-systems provide digital I/O using commercial transceiver chips selected for the frequency bands of interest. A standard low-voltage differential signaling (LVDS) digital interface is used to input up to eight DAEs operating at different frequencies.

A PC/104-Plus compatible Field Programmable Gate Array card, with three low-cost, low-power Xilinx Spartan-3 chips, is used to perform high-speed signal processing operations. The FPGAs can be used to perform communications operations for non-GPS links, as well as code generation and correlation operations needed for GPS satellite tracking. The NAVSYS test bed also uses a commercial off-the-shelf PC/104-Plus processor card based on a Pentium-class, low-power processor. The processor card performs high-level processing and handles user interface and storage.

This paper presents the design of the PC/104-Plus SDR test bed, and describes the SGR which is implemented on the test bed. Reconfiguration capabilities of the SGR test bed along with testing results, and future evolution of the test bed towards SCA compatibility are also presented.

2. NAVSYS SGR TEST BED

The NAVSYS SGR test bed shown in Figure 1 is designed to be flexible to interface with multiple sensors and

antennas, to be reconfigurable to different waveforms, and to be portable for convenient testing.

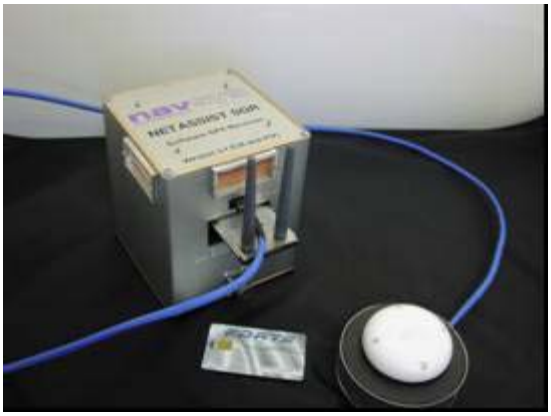

Figure 1: PC/104-Plus SDR Hardware Test bed

Figure 2 shows the high-level core architecture of the NAVSYS SDR test bed. Multiple Digital Antenna Elements provide the RF front-end and are used to digitize and downconvert the signals to baseband. The next stage includes an FPGA card for high speed signal processing. A General Purpose Processor (GPP) provides higher level processing and user or application interface control. In some applications, a security processor is used for crypto functions. This architecture was previously on PC and CompactPCI platforms at NAVSYS prior to migration to PC/104 platforms. An overview of the PC/104 standard along with descriptions of the SDR test bed components is presented in the following sections.

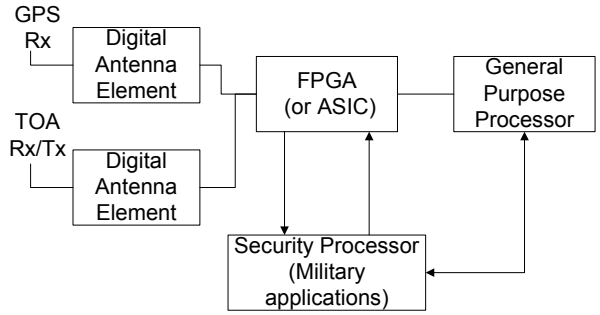

Figure 2 Hardware Test bed Architecture

1.1. PC/104 Standard

The PC/104 Consortium is a group of organizations formed in 1992 to standardize an open architecture for a small, embedded platform that is compatible with IBM personal computer systems [2]. The initial PC/104 standard supported the ISA (Industry Standard Architecture) bus. However, it has evolved to the PC/104-Plus standard which now supports the PCI (Peripheral Component Interconnect) bus. PC/104-Plus is the PCI implementation of PC/104 for I/O functions requiring higher data transfer speeds. It supports a 32-bit multiplexed address/data path operating at PCI localbus speeds of up to 33 MHz yielding a peak bandwidth of 132 MB/sec.

PC/104-Plus systems are similar to standard desktop PCs but with a smaller embedded form factor of approximately 4" by 4" and with lower power consumption. PC/104-Plus boards typically use special stackable connectors carrying standard ISA and PCI bus signals. In addition, a PC/104-Plus system can use the same development tools and operating systems of full-sized PCs reducing the effort and cost of development.

1.2. Digital Antenna Element (DAE)

The DAE is designed to provide a simplified RF front end operating at different frequencies. At present the GPS DAE supports GPS frequencies. A 900 MHz DAE is also being developed for integrated navigation applications using network assistance and time-of-arrival (TOA) capabilities. The DAE offers some attractive features for SDR implementations as outlined below:

- Small form factor of approximately 3" diameter.
- Low power consumption.
- Simplified RF interface that abstracts analog domain to the processing components.
- Currently uses LVDS over standard category-5 twisted pair cable. However, Rocket I/O with HDMI cable will be available for future DAEs.
- LVDS interface allows development of a wide range of antenna elements for different bandwidths/frequencies with a common interface to the FPGA card.
- Sampling rate controllable via far end. Clock can be provided through LVDS pairs for phase-coherent operation, and reduces noise and power introduced by an on-board oscillator.
- Converts analog RF signal to digital domain close to the antenna minimizing cable interference.
- Supports active or passive antenna arrangements.

The GPS DAE depicted in Figure 3, down-converts and samples GPS RF signals and provides a serial digital output to the FPGA card on the test bed which performs GPS code generation and correlation. The GPS DAE is capable of receiving both L1 and L2 GPS signals.

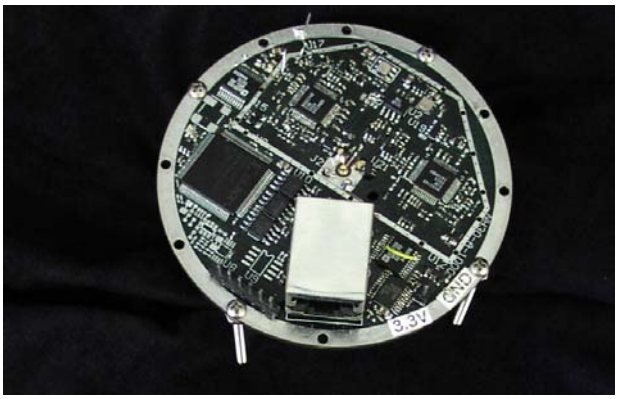

Figure 3 GPS Digital Antenna Element

NAVSYS has also designed a 900MHz transceiver DAE as shown in Figure 6 that can perform receive as well as transmit functions. The received digitized signals are sent to the processing firmware for demodulation. The transmitted digital signals are generated in firmware and software and are up-converted in the 900MHz DAE for broadcast. Both the GPS DAE and the 900MHz DAE are designed to operate from a common sample clock and phase-locked reference Local Oscillator. This requirement assures that the timing between the two signal sources is precisely phase locked. The characteristics of the GPS DAE and the 900MHz DAE are shown in Table 1.

Table 1: DAE Characteristics

	GPS DAE	900 MHz DAE
RF Frequency Range	1575.42MHz (L1), and 1227MHz (L2)	902 - 928MHz
Bandwidth	20MHz	26MHz
Analog IF Center Frequency	15.42MHz for L1, 18.6MHz for L2	15MHz
Sampling Rate	40MHz	56MHz for 26MHz BW, 40MHz for 20MHz BW or less
Bits per Sample	8	14
SFDR		86dBc

A mechanical design of the next generation DAE shown in Figure 4 consists of an RF PCB connected to digital interface board by a 100 pin connector, which is used to transfer the outputs of the A/D and D/A converters. The RF PCB also provides RF control and variable gain stages. The digital interface board can be replaced to accommodate different processing hardware providing the flexibility needed for SDR designs. The design also accommodates different frequencies for the transceiver.

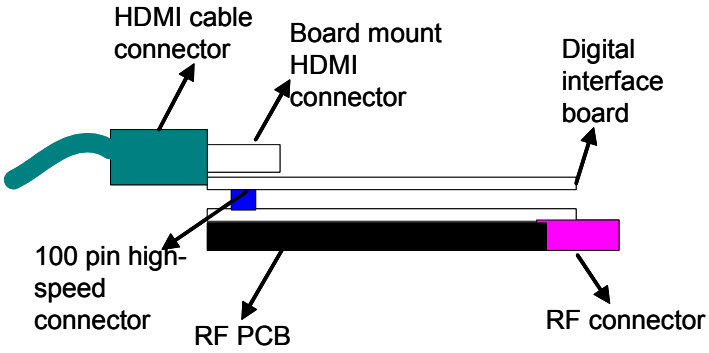

Figure 4: DAE Mechanical Design

1.3. PC/104 FPGA Card

PC/104-Plus FPGA card developed at NAVSYS interfaces with the DAE and can support high speed digital signal processing. The card, shown in Figure 5, contains three Xilinx Spartan-3 FPGAs used to perform high-speed correlations and firmware-based signal processing. Bit-files loaded on the FPGAs are developed using VHDL.

Figure 5: PC/104-Plus FPGA Card

The FPGA card contains a PCI bus chip to provide high speed interfacing between the FPGAs and the processor card over the PC/104-Plus PCI bus. The PCI bus chip also provides interrupt and DMA capabilities. A sustained data rate of 72 megabytes per second has been measured with the FPGA card using DMA data transfer (the theoretical maximum bandwidth is 33 MHz by 32 bits or 133 Mbytes/sec).

The FPGA card also contains an SRAM buffer for storing samples. This sample buffer can be DMAed to the host processor for analysis. This buffer has been used for FFT-based satellite acquisition.

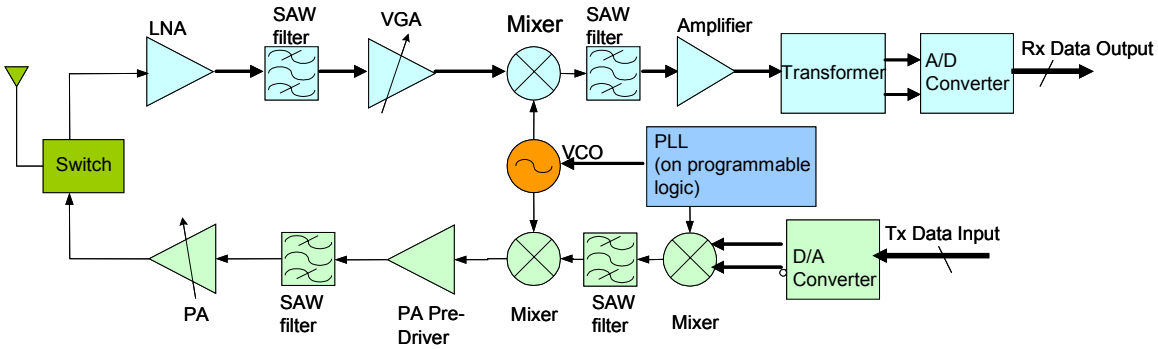

Figure 6: Block Diagram of 900 MHz DAE

1.4. Processor Board

A Pentium-M based processor board interfaces with the FPGA card to provide higher level processing and user interface control. The PC/104-Plus processor card stack has the following specifications:

- 100% PC-AT compatible
- Pentium-M processor to 1.6GHz
- 1024 MBytes SDRAM
- 10/100MBit Ethernet
- EIDE and USB ports
- Low Power ACPI compliant
- PC/104-Plus and PC/104 Expansion
- Available in Extended Temperature
- Standard 3.6in x 3.8in PC/104 form factor
- Low power consumption on the stack, which depends on hardware configuration, and application

The processor card can support multiple operating systems. At present Windows XP and Linux are being used for the implementation of the SGR waveform on the PC/104-Plus test bed. Since most GPS applications require real-time deterministic performance, real-time kernel enhancements to these operating systems are used to support real-time data transfer with direct memory access (DMA). For Windows XP, RTX (real-time extensions for Windows) from VenturCom used to provide this feature while RTLinuxPro from FSM Labs is used for Linux environments. Both provide sub-10μs interrupt latencies. For soft real-time application, any operating system that can run on a Pentium-class standard PC can also run on the PC/104-Plus processor card.

1.5. Integration of Other Sensors

The SGR/SDR test bed can support a wide array of interfaces and sensors. Interfaces such as RS-232, USB, and IEEE 1394 Firewire are being used connect to a variety of navigation and communication sensors. Some of the sensors include an accelerometer, gyroscope, Inertial Measurement Unit (IMU) (Figure 7), barometer/altimeter, and a camera.


Figure 7: MEMS Inertial Measurement

3. NAVSYS SOFTWARE GPS RECEIVER (SGR) ARCHITECTRE

The SGR implements the GPS receiver in software using the output of the correlators on the FPGA card and aids in synchronization of the correlators. The SGR consists of modular high performance object-oriented software that performs real-time satellite tracking and navigation [3]. Each object can input or output data using a messaging framework as shown in Figure 8. Messages can be routed to or from files for post-processing and unit test comparison with MATLAB reference models. Each software object can also be controlled and adjusted using keywords defined in a configuration file. The configuration keywords allow the user to modify the parameters of the receiver algorithms for different operating environments. The firmware models needed for the operation of the SGR can be loaded through the software and in the future will evolve into SCA compatible objects providing true platform independence.

4. SGR APPLICATION AND RECONFIGURABILITY

The Software GPS Receiver architecture developed at NAVSYS is designed to allow rapid prototyping and testing of next generation GPS receiver concepts [4]. The receiver hardware can be configured with multiple

component cards, as needed, depending on the number of antenna inputs and frequencies to be tracked, and the number of receiver satellite channels to be implemented. The firmware is configurable to support different digital signal processing functions, as needed, including spatial processing (e.g. beam-forming), code generation (e.g., C/A or P(Y)) and code correlation and carrier mixing. The modular software architecture allows the user to activate individual software modules, depending on the user's application.

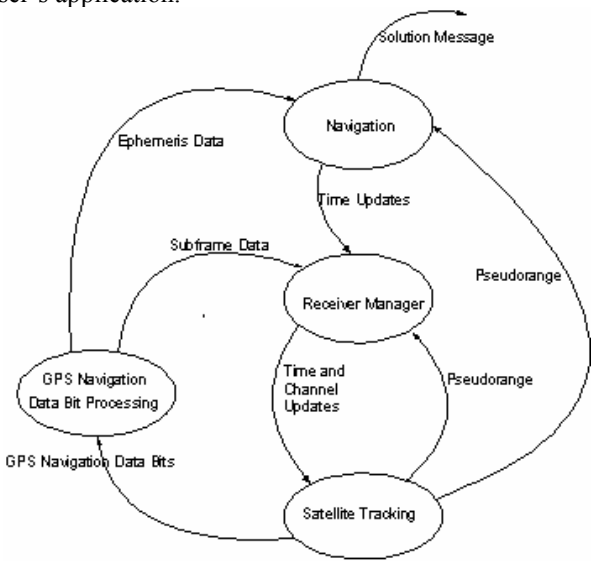

Figure 8: Overview of Software Architecture

This receiver has been used to support a variety of algorithms including digital beam-steering for precision GPS positioning and time observations, GPS anti-jamming tests, and jammer location through direction finding.

Figure 9 shows a configuration of the SGR test bed that includes a GPS DAE, a 900 MHz DAE, an 802.11 data link, and multiple sensors. NAVSYS is developing integrated navigation applications using network assistance on the 802.11 link and time-of-arrival (TOA) capabilities using the 900 MHz DAE.

The SDR test bed is being used to develop the software and firmware to track GPS signals in the SGR and also provide a TOA signal through the 900 MHz DAE when GPS satellites are not visible to certain units. This signal provides TOA aiding by phase locking the broadcast 900 MHz signal to GPS time derived from tracking the GPS time reference signal. The TOA spread-spectrum signal allows multi-channel access and also provides excellent interference rejection properties to other transmitters operating in the ISM band. The data link uses simplex or half-duplex data transmission to allow full use of the 902-928 MHz spectrum for the spread spectrum transmission. Different TOA transmitting channels are identified by the PRN code that they select for the encoding.

Network assistance is used to bolster GPS reception in low signal and degraded signal environments (e.g., tunnels, buildings, under tree canopy, and within proximity to RF transmissions). TOA positioning assistance is also used for areas where GPS reception is impossible using strategically located test bed nodes.

In addition to augmenting GPS reception in degraded signal environments, the sensors on the system can be used to provide comprehensive navigation information. The IMU can be used to derive an inertial navigation solution when aiding is applied either from GPS or another source. The baro-altimeter is used to provide vertical damping to the inertial navigation solution to allow 3-D navigation to be performed during GPS drop-outs. The video camera is used as a truth reference to record the test environment and can also be used to extract surrounding information.

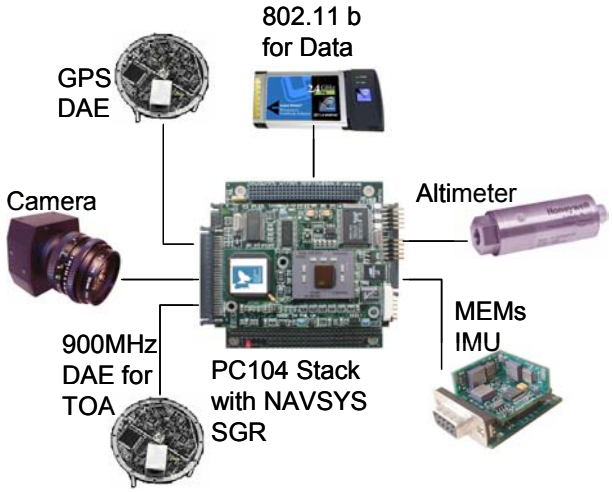

Figure 9 PC/104-Plus SGR Test bed Application Using Multiple Sensors

5. TEST RESULTS

The SGR/SDR test bed was configured to interface with the GPS DAE as well as the 802.11 link. Under this setup, the 802.11 link upon startup was used to synchronize time with a network base station. The base station also provided the GPS almanac and ephemeris information from over the 802.11 link which significantly reduces the Time To First Fix (TTFF). TTFF is the amount of time it takes for the receiver to start providing navigation solutions. Using the above setup the observed TTFF was under 10s. With such network assistance it is also possible to track under significantly lower signal to noise ratios down to nearly 1dB.

6. CONCLUSIONS AND FUTURE WORK

The SGR/SDR test bed provides a flexible platform for implementing integrated navigation systems, with support for other communication waveforms. The key characteristics of the test bed are summarized below:

Reprogramability and Multi-Mode Operation: The SDR test bed consists of reconfigurable hardware that can be configured to implement high speed DSP functions. Further a variety of sensors can interface to the test bed for different GPS receiver configurations. The SGR software can also be configured through simple keywords to tune the tracking loops for different environments.

Flexibility and Hardware Scalability: The reprogrammable nature of the test bed allows introduction of new waveforms through firmware and software modifications. The nature of the PC/104 test bed and the SDR approach simplifies the introduction of additional frequency channels, spreading codes and tracking algorithms. New frequencies are supported by developing a simple Digital Antenna Element RF front end that complies with the PC/104 FPGA board interface.

Use of Standard Hardware and Interfaces: The SGR/SDR test bed uses PC/104 and other PC industry standardized interfaces. The system can be easily upgraded with the addition of PC/104 cards as well as RS-232, USB and IEEE 1394 Firewire components.

Use of Robust, Inexpensive Development Tools: The test bed is composed of low-cost components and builds upon proven PC processor and chipset technology reducing development time and effort.

The SDR test bed provides a flexible platform for development of different waveforms for SDR applications. For the future NAVSYS has charted an evolutionary path for the SGR/SDR test bed towards SCA compliance. The SGR software is modular and object oriented to facilitate its migration to an SCA-compliant architecture in the future. The SGR is also being designed for platform independence using ACE, and implementation options for a lightweight SCA core framework on the stack are being examined. Applications can then configure the stack with the required sensors and algorithms through the core framework which provides a layer of transparency between the application and the underlying hardware. The realization of such a system will be an important step towards incorporating GPS waveforms in software defined radios which in turn can make way for the next generation cognitive radios.

10. REFERENCES

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