A Software GPS Receiver Application for Embedding in Software Definable Radios

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BIOGRAPHY

Kenn Gold is a Product Area Manager at NAVSYS Corporation for the Advanced Systems and Simulation Tools group. His work includes development of spaceborne GPS receivers, integrity monitoring algorithm development, GPS simulator design, and development of Software GPS Radio applications. He holds a PhD from University of Colorado in Aerospace Engineering.

Alison Brown is the President and Chief Executive Officer of NAVSYS Corporation. She has a PhD in Mechanics, Aerospace, and Nuclear Engineering from UCLA, an MS in Aeronautics and Astronautics from MIT, and an MA in Engineering from Cambridge University. In 1986, she founded NAVSYS Corporation. Currently, she is a member of the USAF Scientific Advisory Board, a member of the Interagency GPS Executive Board Independent Advisory Team (IGEB IAT), and an Editor of GPS World Magazine. She is an ION Fellow and was indoctrinated into the SBA "Wall-of-Fame" in 2003.

ABSTRACT

The Software Defined Radio (SDR) is an enabling technology that is being leveraged across a wide range of areas within the wireless industry to provide efficient and comparatively inexpensive solutions to several constraints posed in current systems. Since SDR-enabled user devices and network equipment can be dynamically programmed in software, this allows them to be adapted to provide richer feature sets and introduce advanced new services that provide more choices to the end-user and new revenue streams for the service provider. In this paper, the principle of operation of a Software GPS Receiver, designed for embedding within a Software Defined Radio, is described and test results are presented showing the operation of an SDR test-bed in generating the modernized GPS signals.

INTRODUCTION

The Global Positioning System (GPS) provides positioning and navigation capabilities through processing the L-band, CDMA signals broadcast by the GPS satellite constellation. Currently, GPS chip sets can be purchased for embedding in mobile radios. These are being used to provide position and location-based services to mobile radio users. NAVSYS has developed a Software GPS Receiver (SGR) application that will allow a Software Defined Radio (SDR) to provide GPS positioning information without requiring the use of a separate embedded GPS chip-set. This not only has the advantages of providing a cost effective method for embedding GPS functionality within an SDR, but also allows a forward upgrade path for the next generation GPS signals that are being introduced in the GPS satellite constellation.

NEXT GENERATION GPS WAVEFORMS

In addition to the current C/A and P(Y) GPS signals, the next generation GPS satellites (Block IIR and IIF) will include new waveforms to improve the GPS performance for both military and civil users.

For military users, a new M-code signal is planned to be added to the L1 and L2 frequencies that will improve the robustness of GPS to jamming[1]. This is a Binary Offset Carrier (BOC) code which will also use an encrypted code generation sequence. The spectral characteristics of the 1.023 Mbps C/A code the 10.23 Mbps P(Y) code and the BOC M-code are shown in Figure 1.

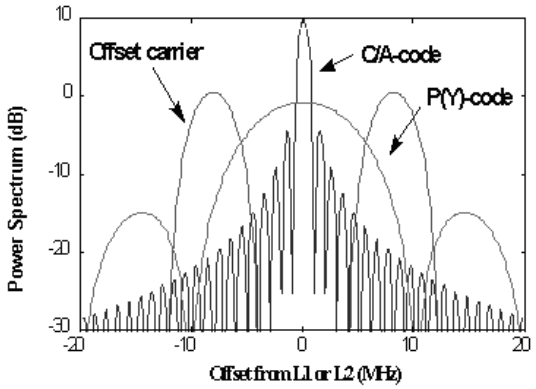

Figure 1 C/A, P and M-code Spectral Characteristics

For civil users, it is planned to add either a new civil PRN code (Lc) or the C/A code on the Block IIR-M GPS L2 frequency[2]. This L2 signal will be available following the launch of the first Block IIR-M modernized GPS satellite in 2004. These satellites have the option of broadcasting either the 1.023 Mbps C/A code or the 2CM and 2CL 511.1 Kbps codes on the L2 frequency. These codes are all generated using a modular-type shift register generator such as is shown in Figure 2.

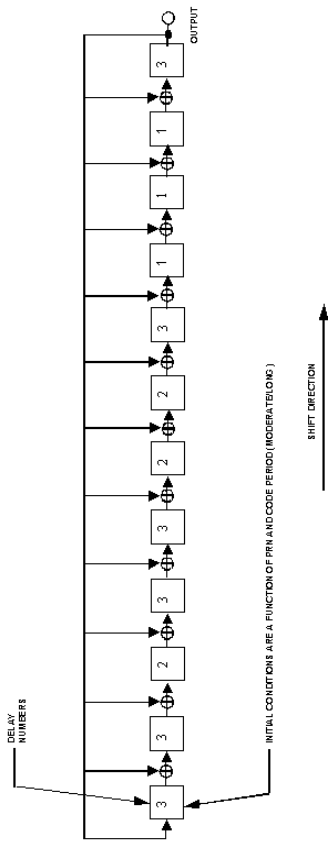

Figure 2 2CM and 2CL Code Generator

The next generation, Block IIF, GPS satellites will also include two additional civil PRN ranging codes that are planned to be transmitted on a third frequency (L5). These are the in-phase code (denoted as the I5-code); and the quadraphase code (denoted as the Q5-code)[3]. Current generation military and civil GPS User Equipment (UE) are not compatible with these new GPS waveforms and will need to be replaced. An advantage of the Software Defined Radio (SDR) architecture for a GPS receiver is that it can be re-programmed to track any of these codes using common hardware, firmware and software components. The different signals that are planned to be provided by the next generation GPS satellite constellation are summarized in Table 1.

Table 1 GPS Legacy and Modernized Signals

SV Blocks	*L1 (1575.42 MHz)*	*L2 (1227.6 MHz)*	*L5 (1176.45 MHz)*
Block II/IIA/IIR	*C/A ⊕ D(t) and P(Y) ⊕ D(t)*	*P(Y) ⊕ D(t) or P(Y) or C/A ⊕ D(t)*	
Block IIR-M	*C/A ⊕ D(t) and P(Y) ⊕ D(t)*	*P(Y) ⊕ D(t) or P(Y) and L2 CM ⊕ D(t) with L2 CL or L2 CM ⊕ D'(t) with L2 CL or C/A ⊕ D(t) or C/A*	
Block IIF	*C/A ⊕ D(t) and P(Y) ⊕ D(t)*	*P(Y) ⊕ D(t) and L2 CM ⊕ D_c(t) with L2 CL or C/A ⊕ D(t) or C/A*	*I5 ⊕ D5(t) and Q5 ⊕ 1 kHz sync*

Notes: *⊕ = Modulo-2 addition*
D(t) = NAV data at 50 bps
D'(t) = NAV data at 25 bps with FEC encoding resulting in 50 sps
D_c(t) = l2 CNAV data and 25 bps with FEC encoding resulting in 50 sps

SOFTWARE GPS RECEIVER ARCHITECTURE

NAVSYS has developed a Software GPS Receiver (SGR) application that is designed to track both the military and civil GPS signals and is planned to be upgraded to allow processing of all of the modernized signals shown in Table 1 once these are available. The architecture that is being used to host the SGR application is illustrated in Figure 3 and includes the following components.

Communication Transceiver Digital Front-End

The Software Defined Radio (SDR) functionality includes an embedded communications capability through its use of a transceiver digital front end (DFE) The

communication receive and transmit functions are handled through an RF transceiver chip that performs the RF to IF downconversion and analog-to-digital (A/D) sampling for the receiver channel and the digital-to-analog (D/A) and IF to RF upconversion for the transmit channel. This interfaces with the firmware embedded within the SDR Field Programmable Gate Array (FPGA) digital signal processor which is used for demodulation and generation of the communication signals. In our current test-bed, this component is implemented using an off-the-shelf RF transceiver chip-set, which operates in the unlicensed International Science and Medical (ISM) 902-928 MHz band..

GPS Digital Front-End

The GPS Digital-Front-End (DFE) components performs the RF to IF downconversion and A/D sampling on the GPS signals listed in Table 1. The DFE can currently accommodate either L1 or L2 signals and a future upgrade is planned to add the L5 signal. This provides the digitized received GPS signals to the FPGA firmware where these signals are processed.

FPGA Digital Signal Processing

The digital signal processing functions needed to control the SDR and perform the GPS signal processing are embedded within the firmware on an FPGA within the SDR. This approach allows the same device to be shared between the communication and GPS signal processing and also allows the SDR to be software upgradeable to accommodate the next generation GPS signals and waveforms. The FPGA is used to perform the high speed code generation and correlation functions needed to acquire and track the GPS signals.

Microprocessor

The host computer is used to control the SDR operation and also run the SGR API that acquires and tracks the GPS satellite signals and computes a navigation solution. A description of the SGR application programming interface (API) is included later in this paper.

Security Processor

The security processor is used for military applications where the SDR also processes the encrypted GPS signals. The SGR API processing is partitioned so that the cryptographic functions can reside on this protected processor. This approach maintains commonality between the military and commercial GPS hardware, firmware and software components while protecting the GPS encrypted signals.

PC-BASED SOFTWARE GPS RECEIVER TEST-BED

The SGR API is designed to be ported onto a variety of test platforms. This includes small portable devices, used for mobile and commercial testing, and also a high-end PC-based architecture. The full PC-based SGR testbed includes the complete set of functions illustrated in Figure 4.

This includes spatial processing (e.g. beam/null-forming), code generation (C/A and P) and code correlation and carrier mixing; a security function where the GPS crypto algorithms needed to generate the secure P(Y) code are implemented; and GPS tracking and navigation processing is performed, including differential GPS and kinematic GPS operation[4]

The modular nature of the PC-based testbed allows it to be easily configured for different applications. The individual components are described below. These are installed in the rack mounted configuration shown in Figure 5.

Digital Front-End Board

The PC test-bed is designed to allow inputs to be provided from multiple antenna elements. This allows the test-bed to perform spatial processing from an antenna array[5], or to receive signals at different frequencies, such as L1, L2 and L5. Each DFE board includes eight separate RF channels, as shown in Figure 6. The input frequency of each individual channel is selected through the front-end filters. The input RF signals are mixed to a 70 MHz IF where they are sampled using a 12 bit A/D converter. The IF filter bandwidth can be selected from 2 to 24 MHz and the sample clock can be adjusted up to 56 MHz. The digitized signal is converted to a low voltage differential signal for transmission to the FPGAs residing on the Correlator Accelerator Card (CAC). The sample rate is selectable based on the DFE front-end bandwidth. The C/A code signals can be accommodated with a narrow-band (2 MHz) filter and sampler. The M-code and L5 signals occupy a bandwidth of 24 MHz and so require a higher sample rate. The DFE board can handle sample rates up to 56 MHz. The sample clock is generated phase locked to the input 5 or 10 MHz clock, and with the L1 and L2 Local Oscillators (LOs).

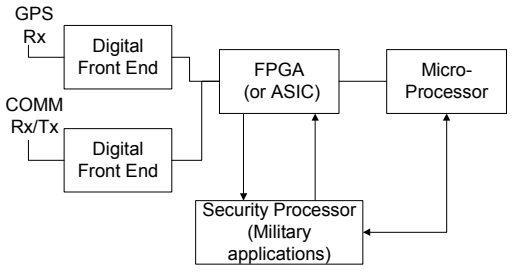

Figure 3 Software Defined Radio Architecture

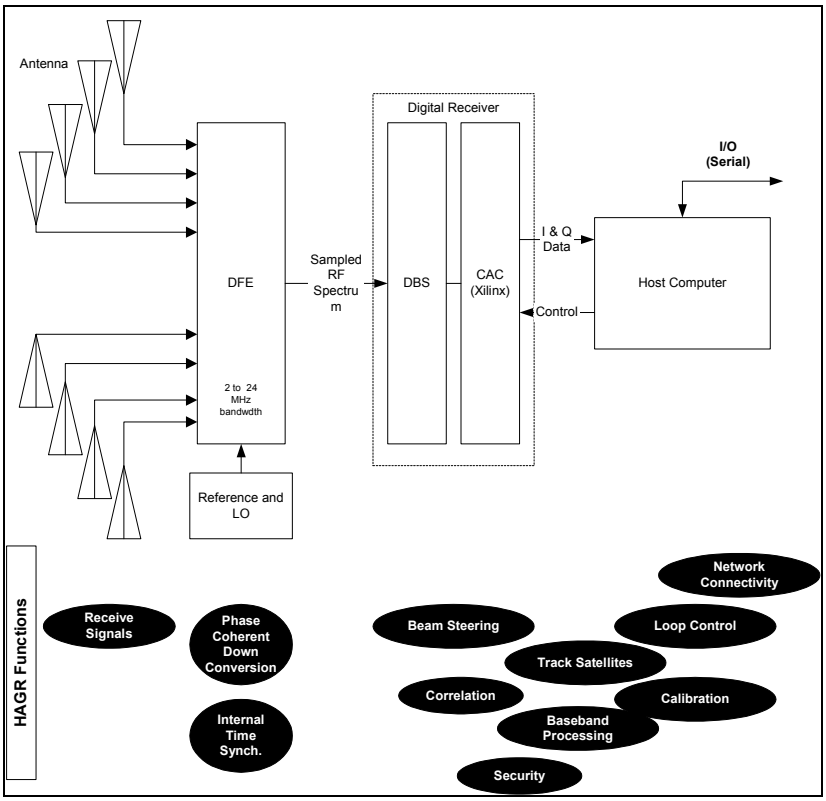

Figure 4 NAVSYS Software GPS Receiver Architecture

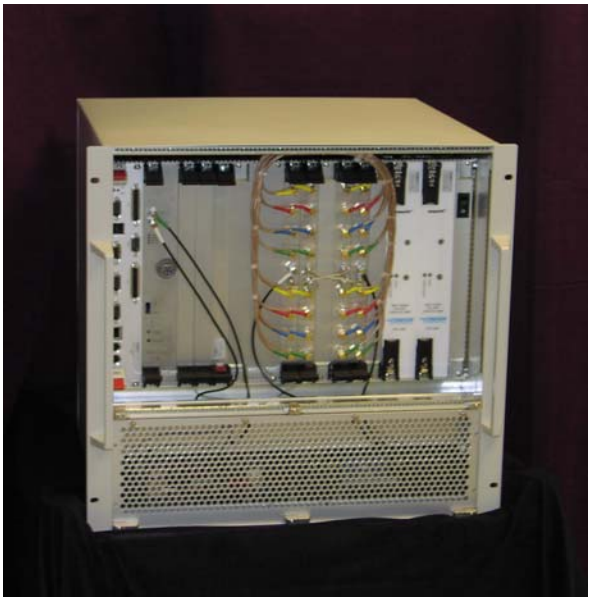

Figure 5 SGR Test-Bed Rack Mounted Configuration

Correlator Accelerator Card (CAC)

The CAC includes the following functions: Code generation, code correlation, carrier mixing and I/Q accumulation. The CAC can also be programmed to perform digital beam-steering when operating with multiple antenna inputs from an array. This functionality is provided for up to 12 satellite channels and is repeated for each code and frequency for every satellite channel tracked. The CAC logic is implemented using Xilinx FPGAs and can be reprogrammed through firmware downloads from the Host Computer. The CAC board layout is shown in Figure 7. The current generation CAC firmware includes C/A and P(Y) (L1 and L2) code generation.

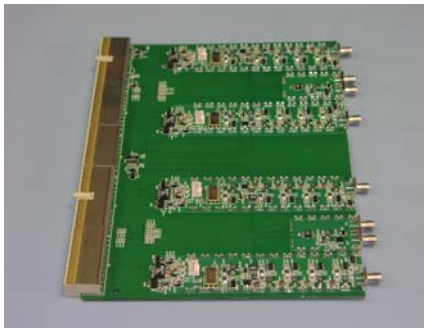

Figure 6 Digital Front End (DFE) Board

Host Computer

A standard PC is used as the host computer. Our baseline configuration is to use an 850 MHz Pentium III CPU with 1 Gigabytes of DRAM and a 40 Gigabyte EIDE hard drive. This can be configured for desk-top, rack-mounted or portable operation. The DFE and CAC cards are installed on the PCI bus of the host computer.

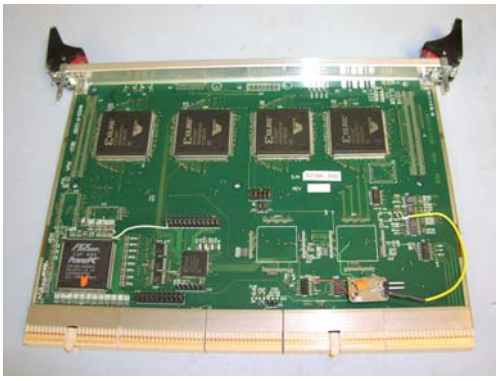

Figure 7 CAC Board

Modular Firmware Design

The CAC Xilinx FPGA firmware used in our GPS software radio uses a set of standard firmware blocks. These blocks include accumulators for correlation, code and carrier NCOs, local bus interfaces, tap registers, and shift registers and counters for PRN generation. Modules are added to the device in a "drag and drop" manner. A binary bit file is generated by the FPGA design tools and saved to disk. This bit file is loaded across the PCI bus to program the devices.

Figure 8 shows the firmware modules used to build a single C/A, P(Y) L1, and P(Y) L2 SV channel. The L1_DATA and L2_DATA busses are the sampled data from the DFE. These busses are generic in the sense that any sampled data may be input into the device, regardless of carrier frequency.

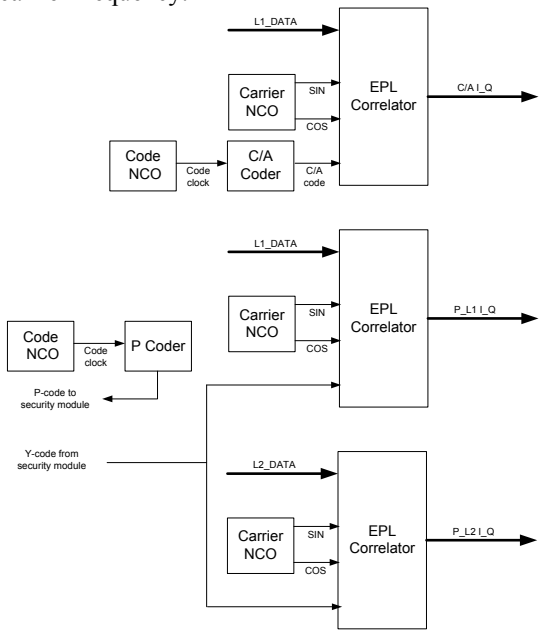

Figure 8 CAC Channel Firmware Blocks

All modules contain control registers that are memory mapped so that they may be controlled by a host computer over a PCI bus. The main blocks in a SV channel are:

- Code NCO – Converts the software downloaded code phase and code frequency values, and produces the code clock for the PRN coders.
- Carrier NCO – Maps the software downloaded carrier phase and carrier frequency values to sine and cosine values to be used for carrier removal.
- C/A Coder – Contains the shift registers and logic to generate the C/A code.
- P Coder - Contains the shift registers and logic to generate the P code. The P code is passed off the FPGA to the security module and returns as Y code.
- EPL Correlator – This block contains the complex multipliers for code and carrier removal. Also included are Early/Prompt/Late shift registers and integrate and dump registers.

To implement a new GPS code a new coder block can be created and dropped into the FPGA design. The new bit file for the FPGA can be loaded across the PCI bus and the software can be modified to provide the necessary control signals. No physical hardware on the CAC board needs to be changed.

OBJECT ORIENTED SGR SOFTWARE DESIGN

The object-oriented Software GPS Receiver application is designed to provide both flexibility and high accuracy performance to allow a common software application to be adapted to meet a broad range of current and future GPS receiver requirements. The SGR software performs the following main functions:

1. Tracks GPS satellites
2. Computes Navigation solutions (standalone and differentially corrected)
3. Interfaces with other computers via Network connections
4. Outputs different data types to log files
5. Operates in Post process with logged data files

The SGR utilizes the latest in object orientated technology to maintain a dynamic, configurable, and highly extensible architecture. The SGR system is comprised of these four major components as shown in Figure 9.

The receiver can be configured dynamically to provide the capabilities necessary to accomplish the assigned operations. These operations may include the selection of code types, number of receiver channels, output data formats and rates, system augmentation types (DGPS, KGPS, positioning, WAAS, etc). While at the same time the different processing modules are completely configurable via the use of "Keywords." These keywords control all the dynamic capabilities within the SGR. Below is a detailed description of each processing element and its capabilities:

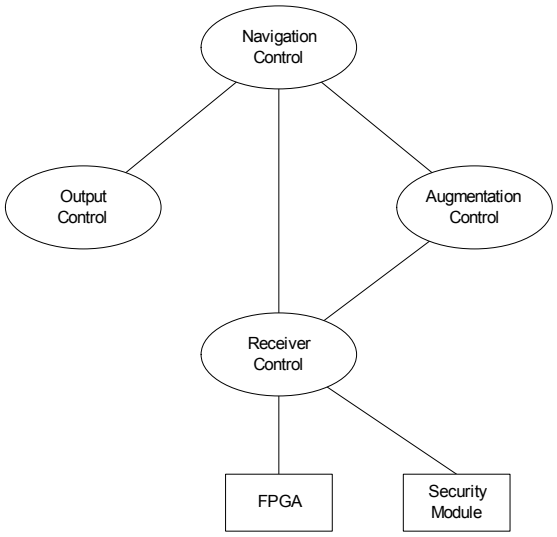

Figure 9 SGR Components

Receiver Control

The Receiver Control processing element provides the following capabilities:

a. Code Tracking loop control
b. Timing control
c. Satellite selection
d. Measurement provision for other modules
e. GPS/WAAS digital data demodulation

This element consists of the following software objects:

a. Track
b. TrackExec
c. ReceiverManager
d. NavData

Augmentation Control

The Augmentation Control element provides the following capabilities:

a. PseudoRange correction
b. CarrierPhase correction
c. PseudoRange correction generation
d. CarrierPhase correction generation

Navigation Control

The Navigation Control element provides the following capabilities:

a. Position determination
b. Fine timing adjustments

Output Control

The Output Control element provides the following capabilities:

a. User display
b. File Storage for Post Processing.
c. File Input for Post Processing

Each Output capability will be unique to a specific application. For example, the user interface would be different for a standard user GPS system verses a Reference Station application.

SGR TEST RESULTS

A major benefit of the Software GPS Receiver is the ability to include measurements from different frequencies. The DFE cards can be used to receive different RF frequencies simply by changing the RF front-end filter and the frequency of the LO input used to mix the signals to the 70 MHz IF. The SGR software is able to track signals at different frequencies simply by changing the Track Module key words. To illustrate this capability, the test set-up shown in Figure 10 was used to insert an L2 signal modulated with C/A code into an L1/L2 DFE card. The GPS software was simply told to look for the C/A code signal at L2 instead of L1. The tracking results are shown in Figure 11. This reprogrammability will be used to test the new GPS satellite signals which will be broadcast from the Block IIR-M GPS satellites schedule for launch later in 2004 (see Table 1). Testing has been conducted to date using M-code test vectors provided by ITT to verify the SGR performance.

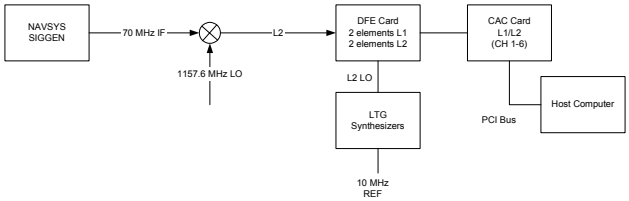

Figure 10 L2 C/A Code Test Setup

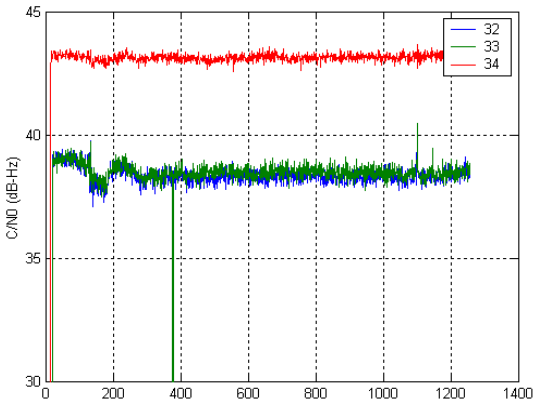

Figure 11 L2 C/A code Tracking

The C/A, P, and M-code signal generated by the CAC using the code generation firmware is shown in Figure 12 to Figure 14.

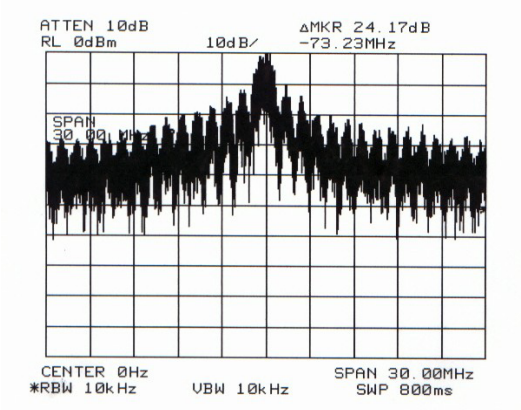

Figure 12 C/A Code CAC output

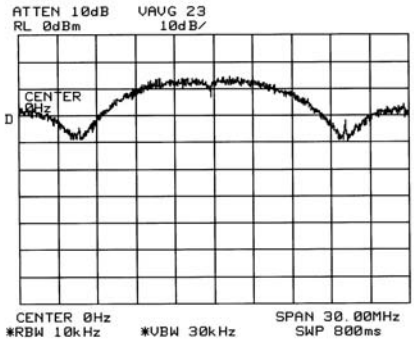

Figure 13 P Code CAC Output

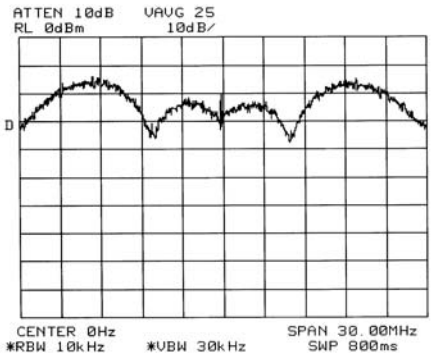

Figure 14 M-code modulation from CAC output

NEXT GENERATION PC-104 SGR TESTBED

NAVSYS is currently developing a small, portable version of our SGR test-bed based on a PC-104 stack architecture. Early prototyping has been completed with this system under various projects. The PC-104 version is shown below in Figure 15, and has the following specifications:

- 100% PC-AT compatible
- Crusoe TM5x00 processors to 800MHz
- 64 - 512 MBytes SDRAM
- 10/100MBit Ethernet
- EIDE and USB ports
- Ultra Low Power ACPI compliant
- PC/104+ and PC/104 Expansion
- Available in Extended Temperature
- Standard 3.6in x 3.8in PC/104 form factor
- Customized Sparton FPGA board

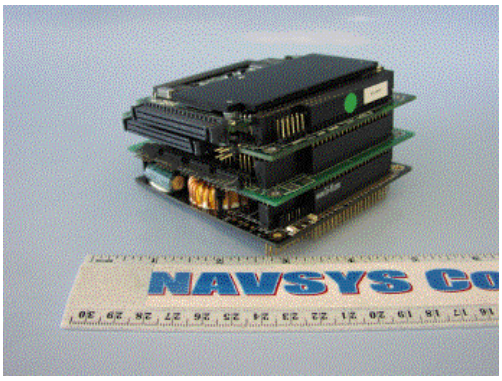

Figure 15 PC-104 SGR PC-104 form factor

CONCLUSIONS

Some of the advantages of embedding the Software GPS Receiver application within a Software Defined Radio are summarized below.

High Performance Operation. The digital signal processing inherent in the software radio approach allows the GPS observations to be derived to high levels of accuracy. The low level access to the GPS signal structure also allows optimized signal processing techniques to be applied to further improve signal processing, such as multipath minimization techniques[6], digital beam-steering and null-steering algorithms and space-time-adaptive-processing (STAP) or space-frequency-adaptive-processing (SFAP) methods.

Multi-Frequency, Multi-Mode Operation. The nature of the software radio simplifies the introduction of additional frequency channels and the tracking of new codes. New frequencies are added through simple changes to the RF-to-digital front-end filters and selection of a new LO. New codes are added through firmware and software modifications.

Flexibility and Upgradeability. The reprogrammable nature of the GPS software radio allows it to be upgraded through firmware and software modifications. This provides a forward upgrade path for adding capability with the modernized GPS satellite signals

Low Cost, Low Power Hardware Implementation. Since both the GPS and communication functions are performed in a single device, the component costs are reduced and power saving is also achieved through sharing of common components

Provides embedded positioning and timing information for mobile services.
Many mobile communication devices desire of have embedded GPS functionality to support mobile value-added location based services such as E-9-1-1 or asset monitoring or tracking. Precise time is also useful for some mobile communication protocols for optimizing operarion and acquiring and handing-off signals. The embedded SGR API provides these capabilities within an SDR.

NAVSYS provides very attractive and flexible licensing terms for the SGR. Licensing is generally based on a licensor's planned production volumes of their product in which the SGR will be embedded. NAVSYS views licensing as a business alliance and will work with their customers to ensure the SGR provides the expected results in the final product. By establishing this type of business relationship, NAVSYS is also available, at additional fees, to provide further unique development of the SGR.

ACKNOWLEDGEMENTS

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