Direct Digital Sampling and Processing of L-Band GPS Signals: A Fully Digital Receiver Architecture

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BIOGRAPHIES

BARRY WOLT

Barry Wolt is a Staff Engineer with NAVSYS Corporation in Colorado Springs, CO, and is chief digital hardware designer for the Advanced GPS Receiver (AGR) described here. He has nine years hardware design experience with five years experience in very high speed digital design utilizing GaAs as well as ECL circuits at frequencies above 500 MHz.

ALISON BROWN

Alison Brown is the President of NAVSYS Corporation, which specializes in developing GPS technology. She has 15 years experience in GPS receiver design and has seven GPS related patents. She has published numerous technical papers on GPS applications and is on the editorial board for GPS World and GIS World magazines. Dr. Brown is currently the Space Representative for the ION Council and Vice Chair for the IEEE Pikes Peak Section.

ABSTRACT

This paper describes the architecture of a digital GPS receiver for use in precision space-based geodesy. The unique design of this receiver allows phase coherent measurements to be made across a broad range of frequencies, enabling measure-ments to be optimally combined from signals on different frequencies, for example GPS L1, L2, and L3, GLONASS, or pseudolites. In addition, the receiver methodology provides precise absolute positioning measurements by maintaining phase coherency between L1 and L2 by direct L-band digital sampling. The receiver uses digital down-conversion by bandpass sampling for a baseband aliased result.

The digitized L-band signals are processed through a digital filter to provide 4-bit in-phase and quadrature-phase samples of the selected frequency for correlation processing. Design of the receiver digital front-end (DFE) provides coherency between the code and carrier phase of the measurements across a 400 MHz bandwidth.

A highly flexible "software receiver" architecture has been developed to allow the receiver to be dynamically reconfigured for different applications. This allows the receiver channels to be used for GPS navigation, ionospheric calibration, attitude determination, or even GLONASS navigation simply through software commands.

In the paper, the AGR hardware topology is discussed with respect to its inherent flexibility that enables tracking any frequencies over a range with only software changes. Test data is also presented to demonstrate the performance of the DFE.

INTRODUCTION

GPS receiver designs have evolved over the last ten years from analog to digital architectures. By reducing the analog functions and transitioning to digital signal processing, significant benefits have been realized in terms of increased performance, and reductions in the size, cost and power requirements. Digital receiver architectures are currently used in all state-of-the-art GPS receivers. The Advanced GPS Receiver (AGR) is the next logical step in the evolution of GPS receivers. The AGR includes a fully digital front-end (DFE) that eliminates a large portion of the analog front-end used in current receivers. This allows further improvements in cost and performance to be realized in GPS receiver designs and also allows the receiver to be used for other functions such as communication and surveillance.

Presented at ION Satellite Division 6th International Technical Meeting, GPS-93, Salt Lake City, September 1993.

Analog GPS Receivers

The architecture of a generic analog GPS receiver is illustrated in 1. This design is used, for example, in the Phase III GPS receivers manufac-tured by Collins. The receiver includes an RF/IF stage that downconverts the GPS signals to a fre-quency close to base-band. At an IF stage, the L1 and L2 frequencies are separated. The Phase III receivers include single channel, two-channel, and five-channel options for different applications. A satellite tracking channel consists of code genera-tion logic (P and C/A code), analog code correlators (two per channel in the Phase III receiver) and mixers to generate In-phase (I) and Quadrature (Q) signals. The I and Q signals are sampled with an A/D converter and processed to close the code and carrier tracking loops for each satellite channel.

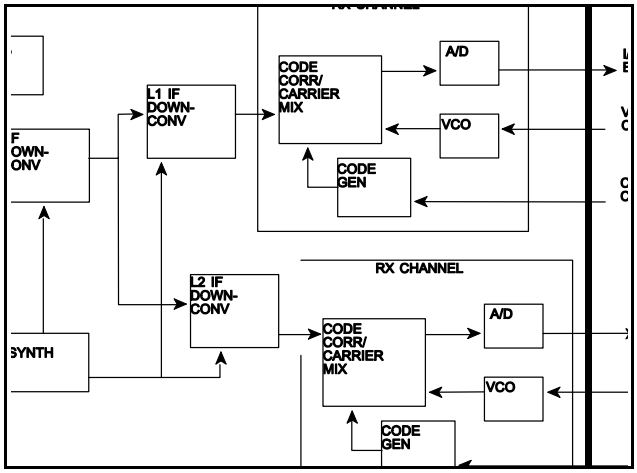

Figure 1 Analog Receiver Architecture

Using this approach, there is a significant increase in the hardware to add extra satellite tracking channels. Because of minor parametric differences in the analog components used, differing delays are introduced in each receiver channel and hence, the satellite observations. This inter-channel bias results in inaccuracies in the pseudo-range obser-vations that have to be calibrated by the receiver.

Digital GPS Receivers

The majority of GPS receivers manufactured today use a digital architecture similar to that illustrated in 2. The receiver includes a fixed frequency analog front-end that performs the downconversion of the L1 (and L2) signals. The I and Q signals are then sampled with an A/D converter before the code correlation and carrier tracking is performed on the individual satellite signals. The code correlation and mixing is performed digitally for each satellite using logical operations to reverse the sign of the I/Q signals and perform complex multiplication to wipe off the estimated satellite Doppler. The accumulated I/Q signals are pro-cessed by the microcomputer to close the digital code and carrier tracking loops in a similar fashion to the analog receiver architecture.

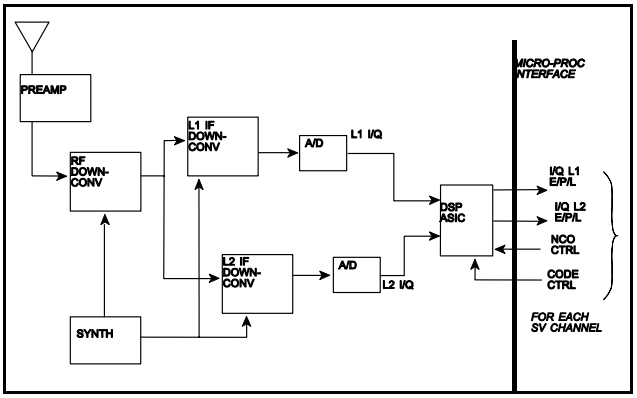

Figure 2 Conventional Digital Receiver Architecture

Thanks to advances in chip technology, it is possible to implement multiple digital satellite channels on a single ASIC. This has resulted in significant reductions in the size, weight, cost and power requirements of a GPS receiver allowing miniaturized, hand-held designs. Since the satellite channels are implemented with high-speed digital logic, the delays in each channel are identical eliminating the inter-channel bias error inherent in the analog design. The digital approach also allows optimal filtering and signal processing techniques to be applied which results in further improvements in the performance and accuracy of the receiver measurements.

Digital GPS receivers are capable of making highly precise measurements of both code (<1 m) and carrier-phase (<1 mm). This performance improve-ment has allowed the development of new naviga-tion methods, such as kinematic GPS, which can be used for high-precision applications such as aircraft landing or geodetic missions. These appli-cations are now placing further demands on receiver performance and reliability that require a next generation receiver architecture.

ADVANCED GPS RECEIVER (AGR)

The AGR has been developed by NAVSYS under an SBIR contract to the Phillips Laboratory, Hanscom AFB. This receiver was designed to be capable of supporting space geodetic missions such as gravity surveying and atmospheric observations. In order to support these missions, new requirements were

placed on the receiver tracking performance and also on the phase stability and coherence of the pseudo-range and carrier measurements on both the L1 and L2 frequencies. To achieve this level of precision, NAVSYS developed a digital front-end (DFE) that replaced much of the analog com-ponents and frequency synthesis required in the current GPS receivers.

The AGR architecture is illustrated in 3. Instead of sampling the downconverted GPS signals, the L-band signals are directly sampled using a high-speed A/D converter. The L1-L2 fre- quency range is selected through analog front-end filters and is amplified prior to sampling. The signal is digitized and a digital filter is used to select the individual frequencies. By under-sampling the L-band signals, the aliasing property operates as a digital down-conversion process. The L1 and L2 I/Q signal outputs are then passed to an ASIC where code and carrier tracking is performed in a similar manner to conventional digital receivers today.

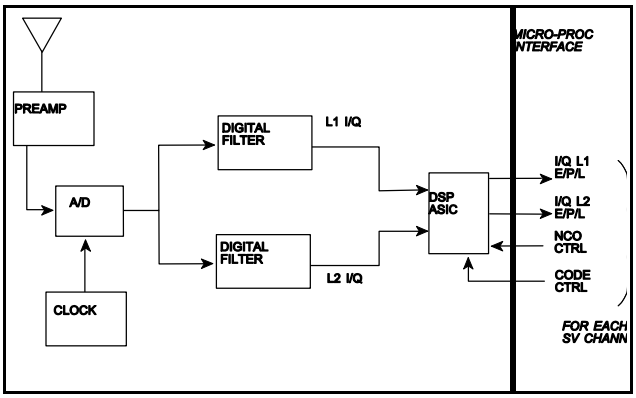

Figure 3 Advanced GPS Receiver (AGR)

The digital down-conversion and filtering applied by the DFE allows the AGR to approach a near-"ideal" receiver architecture. The losses inherent in analog downconversion and filtering are eliminated and phase coherency is maintained on both the code and carrier measurements.

DIGITAL FRONT-END

The AGR digital front-end, illustrated in 4, is comprised of three functional blocks: digitizer, demultiplexer, and precorrelation processor (PCP). The output of the precorrelation processor is 4-bit in-phase and 4-bit quadrature-phase data each for two selected frequencies (e.g. GPS L1 and L2) input to the correlator stage.

The digitizer, or sampling head, samples amplified and bandlimited RF signals at a rate that enables aliasing to baseband to effect digital down-conversion. For GPS L1 and L2 the sample rate is set to 800 MHz (see 5). Sampler bandwidth as well as metastability aperture are critical factors in the selection of a suitable sampler device. The prototype AGR uses monolithic high speed ECL technology for a sampler at a moderately low cost.

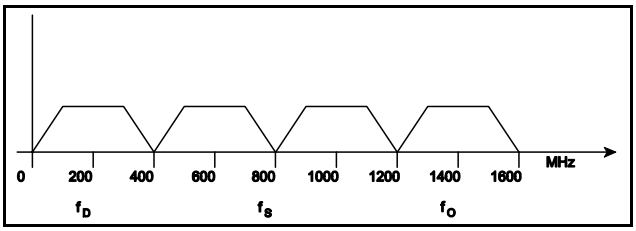

Figure 5 Downconversion

The demultiplexer stage assembles the digital sampler output into 32-bit wide words as well as divides the sample clock by 32 to maintain synchronous operation driven by the sample clock.
The precorrelation processor for the prototype AGR is a two-channel, programmable FIR digital filter that can be configured for passbands at L1 as well as L2 (or any frequency) decimated to 25 MS/s. Outputs are quantized to 4-bits in-phase and 4-bits quadrature-phase.

SAMPLER APERTURE JITTER EFFECTS

The criteria for selecting a suitable sampler device operating in the range of frequencies discussed were primarily a) a sufficiently high bandwidth and b) sufficiently small metastability aperture or sample window. Sample time jitter becomes added amplitude (voltage) noise.

For noise sampling the noise function becomes

$$x_n = n(t_n + \delta_n). \quad \textbf{(1)}$$

where t_n is time at the *n*th sample
δ_n is the jitter noise.

From Rice's representation [1],

$$x_n = n_I(t_n + \delta_n)\cos(\omega_0(t_n + \delta_n)) - n_Q(t_n + \delta_n)\sin(\omega_0(t_n + \delta_n)). \quad \textbf{(2)}$$

where ω_0 is the carrier frequency
n_I is the in-phase component
n_Q is the quadrature phase component.

A truncated Taylor series expansion yields,

$$x_n \approx n_I(t_n)\cos(\omega_0 t_n) - n_Q(t_n)\sin(\omega_0 t_n)$$

$$- \omega_0 \delta_n [\, n_Q(t_n)\cos(\omega_0 t_n) + n_I(t_n)\sin(\omega_0 t_n)$$

(3)

The resulting sample then has multiplicative and orthogonal noise components. It can be seen that the added noise power is proportional to the jitter noise power. The total noise power can then be expressed as

$$\sigma_x^2 = \sigma_n^2(1 + \omega^2 \sigma_\delta^2) \qquad \textbf{(4)}$$

where σ_x^2 is Var(x_n), the variance of x_n
σ_n^2 is Var(n(t)) the ideal analog noise power
σ_δ^2 is Var(δ_n), the variance of jitter noise.

The loss factor due to timing jitter now becomes the ratio of total noise power to ideal noise power expressed as

$$Loss = 10\log_{10}(1 + \omega^2 \sigma_T^2) \qquad \textbf{(5)}$$

where ω is the frequency of interest,
σ_T is the standard deviation of the aperture jitter.

6 shows a curve with correlation loss due to sampler jitter at 1400 MHz center frequency for a pass band including L1 and L2. 6 shows the same result expressing the sampler correlation loss in terms of frequency with a family of curves in the range of measured jitter.

Measured apertures are typically multiples of σ_T (see 6) based on probability of error.

The probability of effective sample time being outside the aperture can be shown as

$$P_E = 2 \bullet Q(K). \qquad \textbf{(6)}$$

The sampler jitter probability can be modeled as the Gaussian Exceedance Distribution given as

$$Q(x) = \int_x^\infty \frac{e^{-t^2/2}}{\sqrt{2\pi}}\, dt. \qquad \textbf{(7)}$$

9 shows the error probability with respect to aperture jitter.

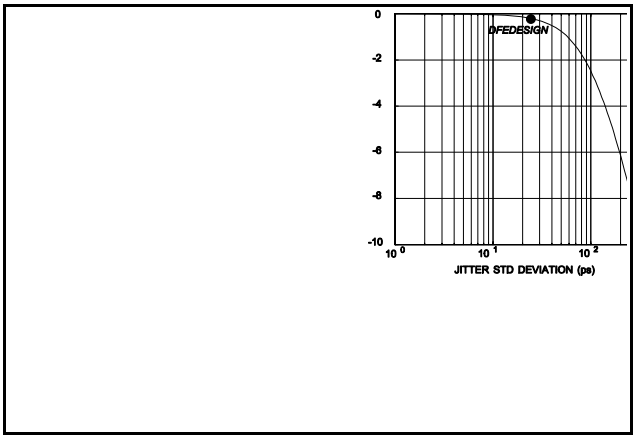

Figure 6 Correlation Loss vs Jitter

SAMPLER JITTER TEST RESULTS

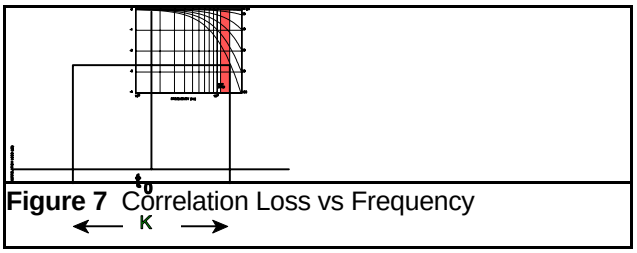

Figure 7 Correlation Loss vs Frequency

Figure 8 Timing Jitter Aperture

Test were run to determine sampler jitter utilizing the test configuration shown in 9. The results were read on a 500 MHz, 1 GS/s digitizing oscilloscope.

The assumption was made that the oscilloscope measurements were on the order of 95% ($\forall 2\sigma$) accuracy of the peak-to-peak jitter due to bandwidth limitations as well as human factors.

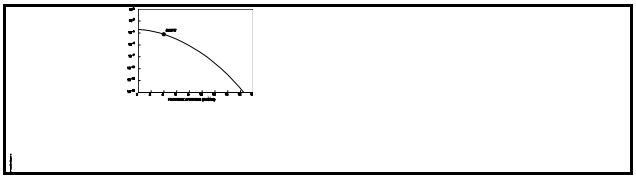

Figure 9 Error Probability vs Aperture

Then,

$$T_J \approx 4\,\sigma_T \qquad \textbf{(8)}$$

$$or, \quad \sigma_T \approx \frac{T_J}{4}.$$

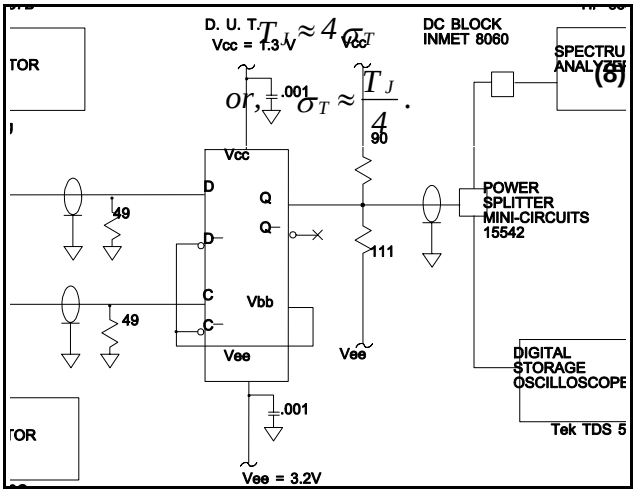

Figure 10 Digitizer Jitter Test

where T_J is the jitter observed.

From the resulting σ_T value, equation 5 determines the loss in the system as shown in 11. The results show loss figures on the order of less than 1 dB (see 6), well within the loss budget for the system.

DIGITAL DOWNCONVERSION

A key feature in the AGR architecture is the elimination of analog components for signal downconversion. By bandpass sampling at 800 MHz, L1 and L2 are converted to baseband for processing at 25 MHz.

Again from Rice's representation, substituting

$$t = nT \qquad \textbf{(9)}$$

into the continuous time model,

$$n(t) = n_I(t)\cos(\omega_0 t) - n_Q(t)\sin(\omega_0 t) \qquad \textbf{(10)}$$

yields the discrete time model,

$$n(nT) = n_I(nT)\cos(\omega_0 nT) - n_Q(nT)\sin(\omega_0 nT). \qquad \textbf{(11)}$$

Now,

$$\omega_0 T = 2\pi\, f_0 T,$$

$$T = \frac{1}{f_s}, \qquad \textbf{(12)}$$

$$\omega_0 T = 2\pi \frac{f_0}{f_s}.$$

where f_0 is the center frequency of interest
f_s is the sample rate.

Letting f_0=1400 MHz, the band pass center frequency for a L1 and L2 receiver, and f_s= 800 MHz yields,

$$\omega_0 T = 2\pi\left(\frac{1400\ MHz}{800\ MHz}\right) \qquad \textbf{(13)}$$

$$= 2\pi\left(\frac{7}{4}\right) = 4\pi - \frac{\pi}{2}.$$

Since multiples of 2 π have no effect, equation 13 reduces to,

$$\omega_0 T = 2\pi\left(2 - \frac{1}{4}\right) = 2\pi\left(\frac{f_0}{f_s}\right) \qquad \textbf{(14)}$$

$$= 2\pi\left(2 - \frac{f_s/4}{f_s}\right)$$

eliminating the 2π multiples,

$$\omega_0 T = 2\pi\left(-\frac{f_s/4}{f_s}\right), \qquad \textbf{(15)}$$

$$\frac{f_s}{4} = f_D = \frac{800\ MHz}{4} = 200\ MHz.$$

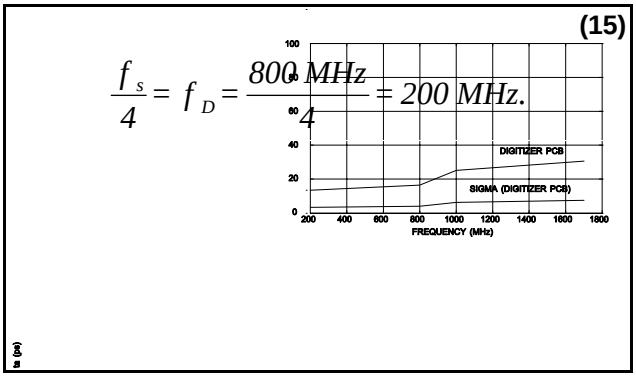

Figure 11 Test Results: System Losses

where f_D is the downconverted center frequency (see

5).

AGR ADVANTAGES

The inherent flexibility of the AGR architecture, and the "near-ideal" receiver design make the AGR easy to reconfigure and ideally suited for a variety of applications.

Implementation Loss

In 1 a breakdown is shown of the AGR implementation loss compared to an "ideal" receiver.

Table 1 Receiver Implementation Loss Budget

	LOSS (dB)
Noise Figure	2.0
Input Quantization (4 bit)	0.1
Sampler Jitter	1.0
Filtering & Aliasing	0.5
Correlator Chip/Misc	0.5
Total Budget	4.1

Because of the almost exclusively digital architecture and the minimal loss in signal processing, the implementation loss can be reduced to a negligible level in the AGR design. This trans-lates to improved tracking performance and improved measurement reliability. For example, a 1 dB improvement in the receiver implementation loss over conventional digital receivers gives nearly an order of magnitude reduction in the probability of a carrier cycle slip occurring. Minimizing cycle slips is an important design factor for kinematic GPS, and is a key requirement for applications such as aircraft precision approach and landing.

Software Receiver

To fully exploit the performance and adaptability of the AGR, a "software" receiver architecture was adopted. The design philosophy was to provide a detailed command structure to the user to allow all of the receiver initialization and signal processing parameters to be adjusted. This allows the receiver to be reconfigured for different applications, to track different types of signals, or to implement new signal processing techniques without any changes to the firmware or software.

2 shows some sample command parameters. These allow, for example, the AGR digital filter frequencies to be selected, the satellite or spread-spectrum signal type to be identified and the tracking loop bandwidths and data rates to be adjusted. The command parameter interface also permits other software to interact with the AGR, for example to dynamically adjust the tracking loops based on current signal strength, jamming or vehicle motion.

Table 2 Tracking Commands and Parameters

Doppler_search	Type of search pattern (expanding or linear)
Doppler_range	Frequency range of doppler search
Data_rate	Length of a data bit
T_1	Initial acquisition threshold (10 ms correlation)
T_2	Verify threshold (100 ms corr)
T_3	Correlation loss threshold (100 ms corr)
T_AFC	Threshold on AFC locksum to change state
T_hysteresis	Difference between state enter and exit thresholds
T_lock_sum	Threshold on locksum
T_bit_sync	Threshold for exiting state based on locksum
T_phase_err	Threshold on RMS error to enter state
T_mid_space	Threshold on RMS code jitter to enter state
T_mid-back	Threshold on RMS code jitter to fall back from state
T_11	Codeless acquisition threshold
T_12	Codeless correlation threshold to maintain acquisition
Sig_threshold	Threshold on 100 ms integrated IQ square for current tracking state
Sig_sqr_max	Max limit on signal measurement
Sig_sqr_min	Min limit on signal measurement
Alpha_3-6	Gain controlling time constant of locksum for specified state
Alpha_RMS	Gain controlling time constant of RMS error measurement
Alpha_noise	Gain controlling time constant of SNR measurement
Alpha_code_err	Gain controlling time constant of code jitter
Alpha_code_RMS	Gain controlling time constant of code jitter RMS
B_DLL	Bandwidth of DLL (Hz)
B_FLL	Bandwidth of AFC loop (Hz)
B_PLL	Bandwidth of PLL (Hz)
B_IQ	Bandwidth of IQ loop (Hz)
Codeless_end_state	Codeless tracking end state

Multi-Function/Reconfigurable Design

The AGR architecture can be configured to serve a variety of different applications, as illustrated in 12. Because of the digital nature of the design, it is possible to separate the DFE and digital signal processing (DSP) functions. This allows multiple DFEs to be integrated with multiple DSPs which provides a new level of flexibility in configuring receiver architectures. Where appro-priate (e.g. for space applications), the same com-ponents can even be reconfigured through switching interfaces and software to serve totally different on-board functions.

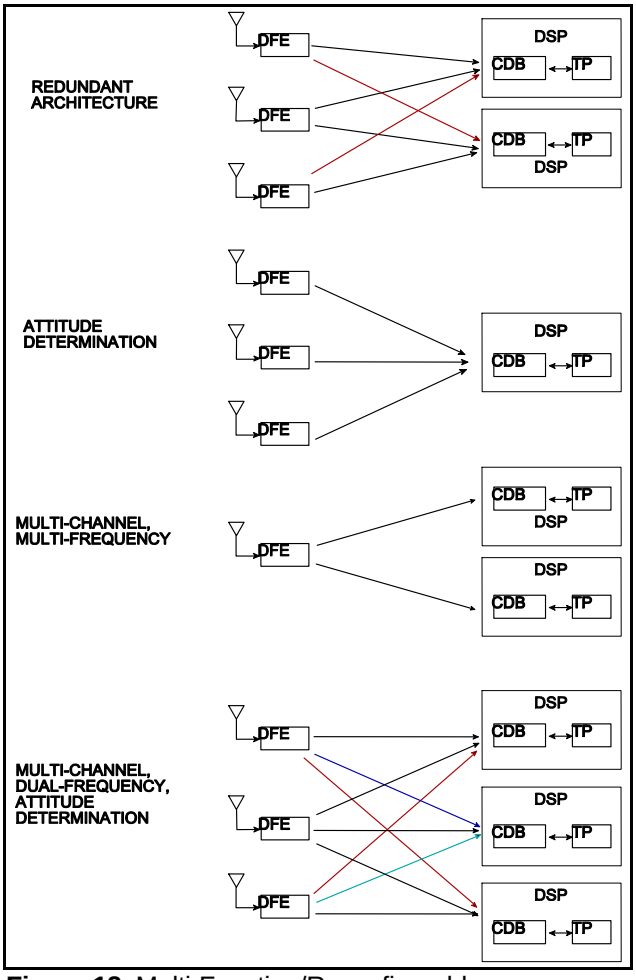

Figure 12 Multi-Function/Reconfigurable

For space and aircraft applications where equip-ment reliability is important, the AGR can be con-figured with multiple DFEs and DSPs to give a redundant architecture, as illustrated in 12. This allows single point failures of any one component to occur without impacting system performance.

By combining the signals collected from multiple DFEs, it is possible to perform optimal signal processing of the relative delays and carrier phases between antennas. This allows attitude to be determined in addition to the other navigation functions. The digital design permits more precise attitude measurements to be made than previously possible.

To increase the numbers of channels in the AGR, multiple DSPs can be integrated with a single DFE. This allows the receiver to grow to 12-channel L1/L2 when required. Finally, by allowing dynamic switching between different DFEs and DSPs, a multi-function receiver architecture is possible that can be reconfigured under software control to serve all of the above functions.

CONCLUSION

In 3 a list of the AGR features and benefits is provided for a variety of the applications that this receiver can serve. These include space, military and commercial markets. The AGR design is not only valuable as an end-product for these appli-cations but is proving to be useful as a test-bed for new digital signal processing techniques that are enhancing performance levels in communication and navigation applications.

The Advanced GPS Receiver is being developed under an SBIR contract to Hanscom AFB. NAVSYS is also under contract to ARPA to test the AGR for use in an autolanding system for Unmanned Autonomous Vehicles (UAVs). Under the next phase of the AGR development, the DFE will be reduced to a single chip and a miniaturized version of the receiver will be produced.

REFERENCES

[1] A. Papoulis, *Probability, Random Variables, and Stochastic Processes*, Second Edition (New York: McGraw-Hill, 1984).

[2] A. Brown, "Advanced GPS Receiver for Space Applications," SBIR Final Report, Hanscom AFB PL-TR-91-2251, Oct 1991.

Table 3 Benefits of AGR Architecture

AGR FEATURES	Digital Front End	Multi-Freq Tracking	High Rate/ Accuracy Meas	Coherent Code/Carrier Tracking	"Software RX" Multi-Function Design	P/Y-Code (Upgrade)	Codeless L2 Tracking
SPACE							
LAUNCH VEHICLE G&C	X		X		X		
ORBIT DETERMINATION	X		X		X		
ATMOSPHERIC OBSERVATIONS	X	X	X	X	X		X
REAL-TIME DGPS	X	X			X		
ATTITUDE CONTROL	X		X		X		
MILITARY							
PRECISION APPROACH & AUTO-LANDING	X	X	X	X		X	
ANTI-JAMMING	X	X					
COMMERCIAL							
CAT II/III PRECISION APPROACH	X	X	X	X			X
IONOSPHERIC OBSERVATIONS	X	X		X			X
GEODETIC OBSERVATIONS	X						X
PRECISE TIMING	X		X			X	X