

# Dynamic Reconfiguration in a GNSS Software Defined Radio for Multi-Constellation Operation

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## BIOGRAPHY

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## ABSTRACT

Recent advances in the US GPS constellation have resulted in additional signals being made available for both military and civil applications. The modernized GPS signal structure now includes signals broadcast on three frequencies with both the legacy GPS modulation codes, additional civilian codes, and also additional military codes on L1 and L2. In the next few years, GNSS users will also be able to access increasing numbers of new signals from other satellite constellations, including the European Galileo, the Russian Global Navigation Satellite System (GLONASS), the Japanese Quasi-Zenith Satellite System (QZSS), the Indian GPS Aided Geo Augmented Navigation (GAGAN) and the Chinese Compass Navigation Satellite System.

Historically, GNSS receivers have been designed with dedicated channels each capable of tracking only a single satellite code. As the number of codes and frequencies increase, the demands on a conventional GPS receiver get higher. Moreover, to track the different signals broadcast by other GNSS satellite systems, even more channels would be required to be set up to track their new codes. The increase in the number of channels using a conventional receiver design would also result in increased device size and correspondingly higher power operation. In this paper,

we describe a GNSS Software Define Radio (SDR) architecture that allows for dynamic reconfiguration of the SDR channel resources to track different GNSS satellite codes and frequencies. With this approach, the flexibility of the SDR can be leveraged to implement a full-function GNSS receiver capable of leveraging any of the GNSS signals without requiring massive numbers of parallel channels to operate.

## INTRODUCTION

Historically, GNSS receivers have been designed with dedicated channels each capable of tracking only a single satellite code. When operating using only the C/A code signals from the GPS satellites, this has been manageable and GPS chip sets routinely allow tracking of twelve or more satellites at the same time. As the number of codes and frequencies increase, the demands on a conventional GPS receiver get higher. With the GPS satellites alone, a next generation receiver could be required to operate on three frequencies each using a different code which would require triple the number of channels when using a conventional receiver design. Moreover, to track the different signals broadcast by other GNSS satellite systems, even more channels would be required to be set up to track their new codes. The increase in the number of channels using a conventional receiver design would also result in increased device size and correspondingly higher power operation.

In order to obtain a good navigation solution, it is only necessary to operate enough tracking channels in a GNSS receiver to obtain sufficient satellites in view to achieve good geometric dilution of precision. That generally only requires between six to twelve Global Navigation Satellite System (GNSS) signals. In this paper, we describe a GNSS Software Define Radio (SDR) architecture that allows for dynamic reconfiguration of the SDR channel resources to track different GNSS satellite codes and frequencies. With this approach, the flexibility of the SDR can be leveraged to implement a full-function GNSS receiver capable of leveraging any of the GNSS signals without requiring massive numbers of parallel channels to operate.

## GLOBAL NAVIGATION SATELLITE SYSTEMS

While GPS provides the most consistent coverage today on a global basis, there are already in operation a large number of other Global Navigation Satellite Systems. It is common already for GPS chip set vendors to support both GPS and the Regional Navigation Satellite Systems (RNSS) which share common codes on the L1 (C/A) and the L5 frequencies. RNSS systems are already being operated by the US (WAAS), Europe (EGNOS), Japan (MSAS), India (IRNSS) and China (Beidou). The number of GNSS and RNSS satellites is steadily increasing as the system providers execute their launch programs. As shown in Figure 1, over 90 satellites are projected to be launched. Figure 2 shows the current numbers of GNSS satellites visible at any location in the world. This shows that the greatest growth in satellite availability is over Asia where as many as 35 different GNSS and RNSS satellites can be in view at any time.

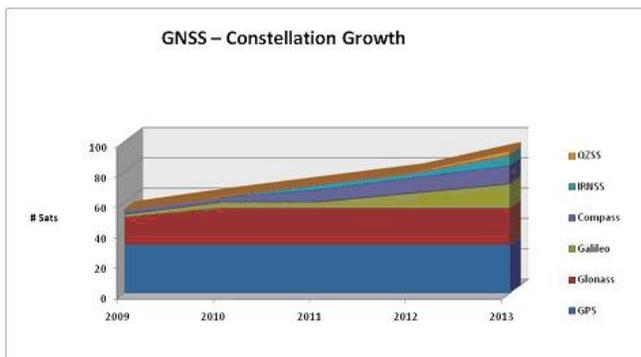


Figure 1 GNSS predicted satellite growth to 2013<sup>[1]</sup>

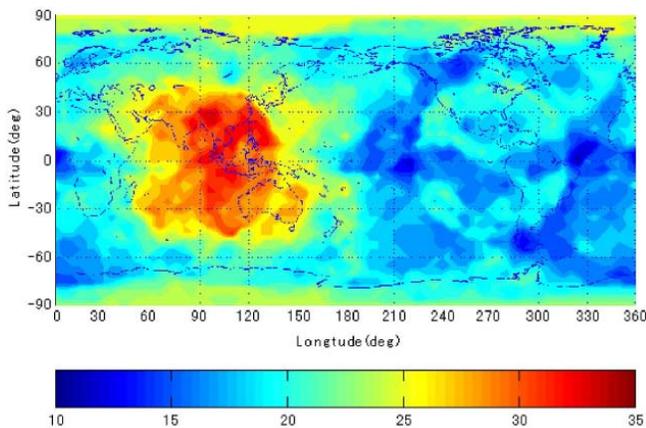


Figure 2 GPS+GLONASS+Galileo+COMPASS+RNSS +QZSS Satellite Visibility<sup>[2]</sup>

With the increase in the number of GNSS constellations there is also an increase in the number of different codes that GNSS chip sets need to be able to handle. With prior chip set designs, commercial vendors focused on channels that could track only the C/A code or sometimes also the P(Y) code using codeless techniques. Current generation

GPS chips can include up to 48 channels for satellite signal acquisition. As chip sets evolve that can track more GNSS signals with different codes either additional channels are needed or larger channels with the ability to handle multiple GNSS signal types. This going to affect the size, weight and power of future GNSS chip sets when using conventional ASIC technology.

The legacy and modernized GPS signal structure is shown in Figure 3. Future GPS users will have access to additional signals on the L1, L2 and L5 frequencies (L1c, L2c, I5, Q5) which will require additional channels to track.

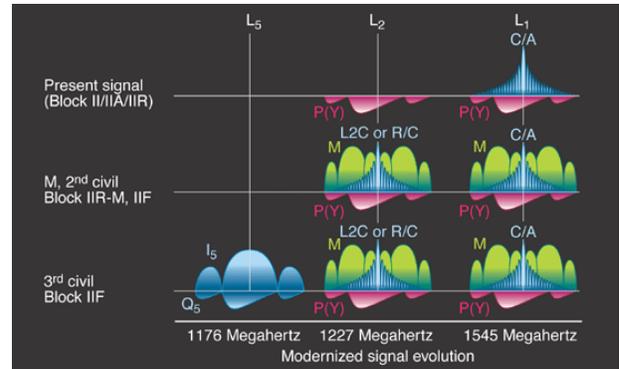


Figure 3 Modernized GPS Signal Structure

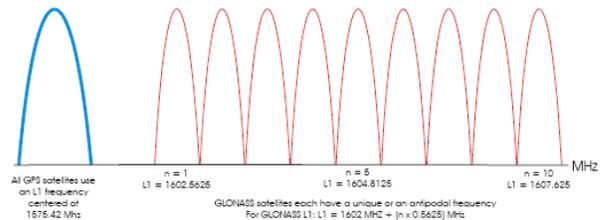
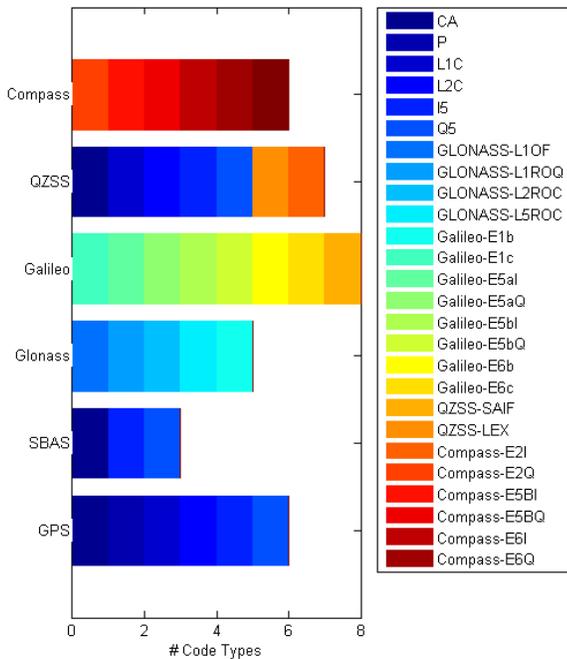


Figure 4 GLONASS L1 FDMA Signals<sup>[3]</sup>

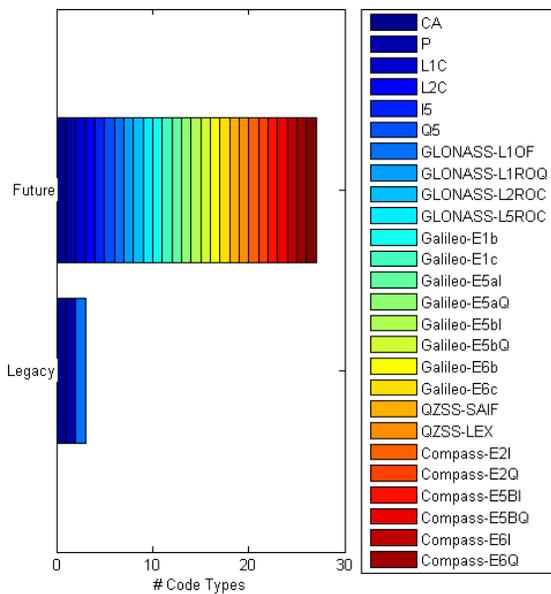
The GLONASS legacy satellites broadcast FDMA signals (see Figure 4) on the L1 and L2 bands<sup>[4]</sup>. Civilian GPS receivers track the L1 and L2 “Open” Signal (L1OF and L2OF) while military receivers can access the high precision “S” obfuscated signal (L1SF and L2SF). The first GLONASS-K satellite, which is part of the GLONASS upgrade program, was launched in February 2011. The GLONASS-K satellites will transmit additional navigation signals to improve the system’s accuracy including additional civilian CDMA signal that will be transmitted in the L1, L2, L3 and L5 bands (L1ROC, L2OC, L3OF, L5ROC).

The Galileo satellites also broadcast multiple signals on the L1, L5 and L6 bands (E1-B, E1-C, E5a-I, E5a-Q, E5b-I, E5b-Q, E6-B, E6-C) using a combination of BPSK and BOC modulation<sup>[5]</sup>. Figure 5 shows the combined GPS, GLONASS and Galileo signals.





**Figure 8 Code Types by GNSS Constellation**



**Figure 9 Comparison of Legacy and Future GNSS Civilian Code Types**

While it is necessary to be able to track any of these different GNSS signals in order to benefit from the increased coverage and availability provided by these multiple constellations, it is not necessary to track all of the visible GNSS satellites in order to obtain a good navigation

solution. Adequate dilution of precision can generally be obtained with six or more GNSS satellites being tracked so long as they are selected from the visible set of satellites to provide optimum geometry. Since only two frequencies are needed to observe the ionospheric delay, a GNSS receiver could provide accurate navigation with 12 channels capable of tracking any satellite signal (code or frequency). While modern receivers include larger number of channels, which can assist in speeding acquisition, next generation receivers that can leverage network assistance to facilitate acquisition, could operate with significantly fewer numbers of channels if all of the GNSS signal types could be accommodated in a flexible channel design. Rather than building a massive channel including all code type combinations, an alternative design enabled through Software Defined Radio architectures is to instead use dynamic reconfiguration to allow a conventionally sized channel to be reconfigured to accommodate any code type.

### GNSS SDR DESIGN

NAVSYS Corporation is currently leveraging our prior GPS SDR development efforts<sup>[9, 10, 116]</sup> to design a miniaturized SDR architecture with low-power design features and dynamic reconfiguration of the receiver channels to allow different GNSS frequency bands and signal codes to be processed by each channel. The SDR design being developed is flexible enough to cover the GNSS frequency bands. The design is being tested first with the GPS modernized signals but is flexible enough to handle in the future the signals from other GNSS satellite systems.

As illustrated in Figure 10 and Figure 11, the GNSS SDR uses multiple RF channels to receive the L1 (1575.42 MHz), L2 (1227.6 MHz) and L5 (1176.45 MHz) signals. The digital outputs from each of these RF channels, termed Digital Antenna Elements (DAEs), are then provided to the SDR baseband processor. If any RF channel is not being used it will be disabled to save power. The GNSS SDR is currently being upgraded to include a reprogrammable RF front-end that would allow any of the GNSS signal frequencies to be tracked by the SDR channels.

The entire receiver baseband processing is being implemented on a single Xilinx Virtex-6 FPGA (Field Programmable Gate Array). The FPGA is initially loaded from external flash memory with a base configuration to enable communication to a host input device. The user would then be able to select any combination of GNSS codes to be tracked by the six receiver channels. Utilizing Xilinx dynamic partial reconfiguration, the receiver channels are loaded from external flash memory and configured by the host to acquire and track specific satellite signals.

If the user decides to track different GNSS codes, that change can be made at any time. Once the system receives the command to reconfigure from the host, the FPGA will read the required partial reconfiguration bit files from external flash RAM and use that to configure the selected channel. RF channels and encryption key management modules will be enabled or disabled as needed. Tracking operations of the other five channels will not be affected by the reconfiguration.

At initialization, the new receiver channel will be handed accurate knowledge of time that will allow it to begin tracking satellites extremely quickly. This will be done without powering down the system that would result in a “cold start” state of satellite tracking.

In Figure 10, a conventional C/A code operation is shown where all of the channels are set to perform C/A code correlation using only an L1 RF Channel (termed Digital Antenna Element). In Figure 11, the SDR configuration is shown where the resources are shared between tracking satellites on the L1 C/A code and also on the L2C code. The GNSS SDR channel could equally well be configured to switch to any GNSS code/frequency pair allowing tracking of the optimum satellite set for navigation with an efficient channel design.

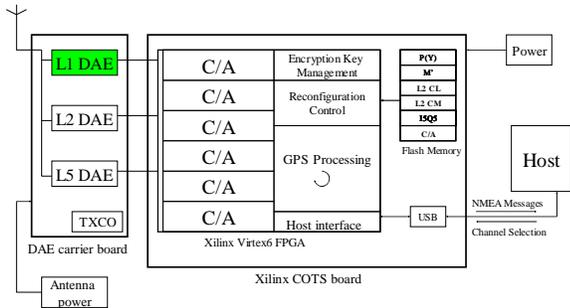


Figure 10 Default configuration using L1 C/A code

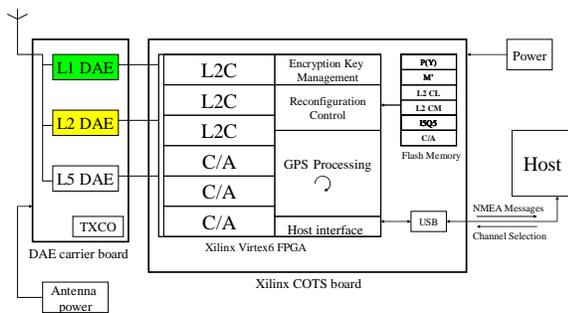


Figure 11 Change to L1 C/A and L2C tracking

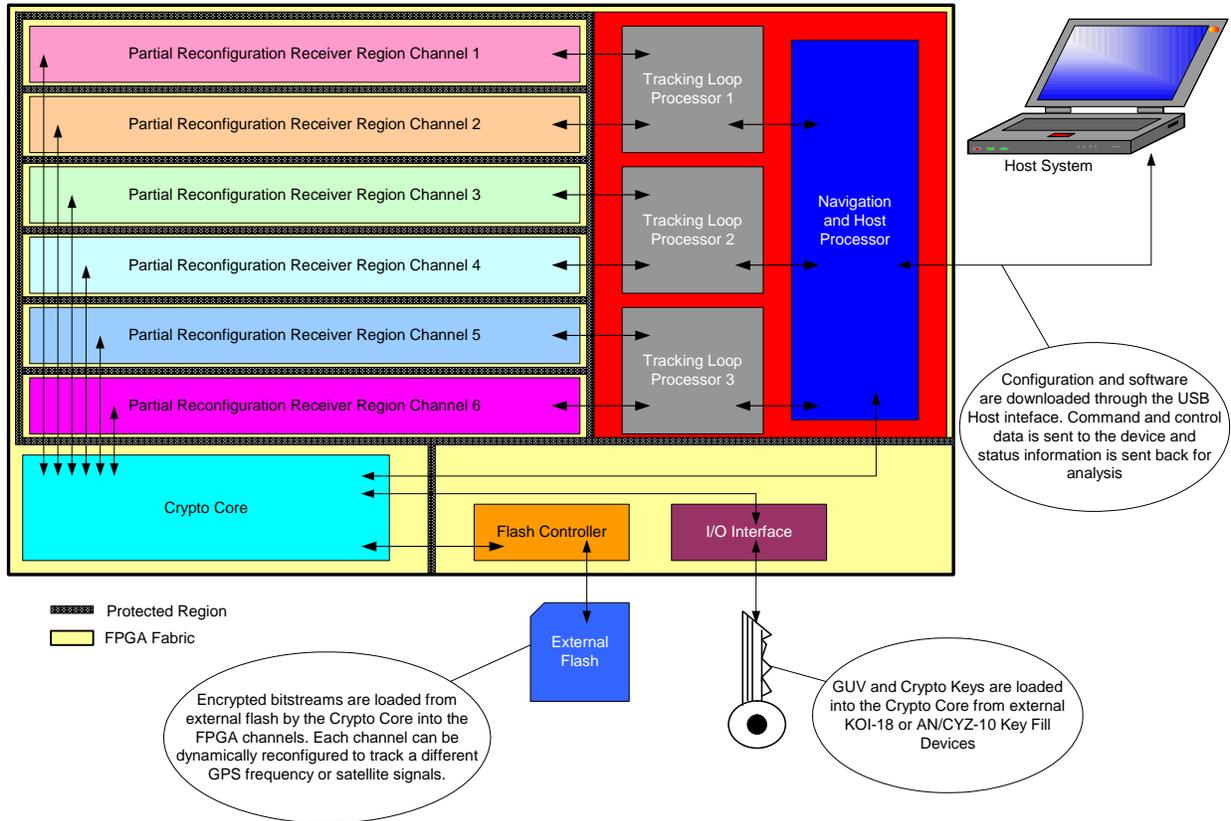
## XILINX BASEBAND PROCESSOR DESIGN

The Xilinx Baseband Processor design is illustrated in Figure 12. In this design, a partial reconfiguration region is established for each GPS processing channel. Each processing channel follows a common design consisting of signal selection, signal and code NCOs, GPS code generators, correlation channels, and a register interface. The signal selection code at the channel front end determines which RF front end (L1/L2/L5) is processed and which GPS crypto variable is used for the military code generation. The number of correlators used in each channel depends on the complexity of the signal being processed by that channel.

A register interface between the partial reconfiguration channel and the tracking loop processor provides the means for the tracking loop processor to set up NCOs, code generators and signal selection. It is also used to transfer correlator results to the tracking processors. The register interface for each channel is mapped into the memory of one of the tracking loop processors in the central section. The tracking loop processors are Xilinx MicroBlaze instantiations. Currently, two tracking channels are handled by each of three MicroBlaze processors. Using a memory-mapped register interface provides a simple and efficient data path between the channel hardware and the tracking processor. Each tracking loop processor handles two tracking channels and communicates with the navigation processor and crypto core using serial interfaces. A fenced area on the Xilinx chip is used to store GPS keys and perform the GPS crypto variable generation.

An additional MicroBlaze processor in the central section implements the GPS navigation computation and also provides the host interface. Navigation can use GPS navigation message data extracted from satellite signals or provided via the host interface if the host has a network connection. The host interface is USB with a simple NMEA-format command set that is used to configure/control the receiver and to obtain the PVT solution from it. If the host is an SCA-based Joint Tactical Radio System (JTRS) radio then a small SCA component running on the host’s red side provides an adapter between the USB interface to the GNSS device and the SCA applications on the JTRS radio.

The internal fencing is built from unused configuration logic blocks (CLB). In the fence, no routing or logic can exist. This provided at least three physical failures before the separation boundaries are breached<sup>[12]</sup>.



**Figure 12: Xilinx Baseband Processor Design**

## DYNAMIC RECONFIGURATION

Using Xilinx’s dynamic reconfiguration capability<sup>[8]</sup>, each of the FPGA channels in the GNSS SDR can be dynamically reconfigured to track a different GPS frequency or satellite signal. The common base configuration is programmed into the FPGA when it first boots from the flash memory. The GNSS SDR user can then decide what processing will be required in each of the six reconfigurable channels. The appropriate FPGA bitstream is then loaded into each of the dynamically reconfigurable areas from the flash memory. The size of each of the reconfigurable regions is fixed and determined by the complexity of the largest processing algorithm estimates of the required FPGA resources for each of the supported GPS signal types. Figure 12 illustrates how the FPGA bitstreams are loaded into the dynamically reconfigurable areas. The partial bitstream loading is done through the Xilinx Internal Configuration Access Port (ICAP)<sup>[9]</sup>. This internal port allows for the reconfiguration image to be decrypted and verified before being applied without ever leaving the FPGA where it could be tampered with. In the current family of Xilinx FPGAs, the ICAP interface is a 32 bit bus operating at a maximum frequency of 100MHz. This yields a maximum throughput of 3.2Gb/second. This will allow

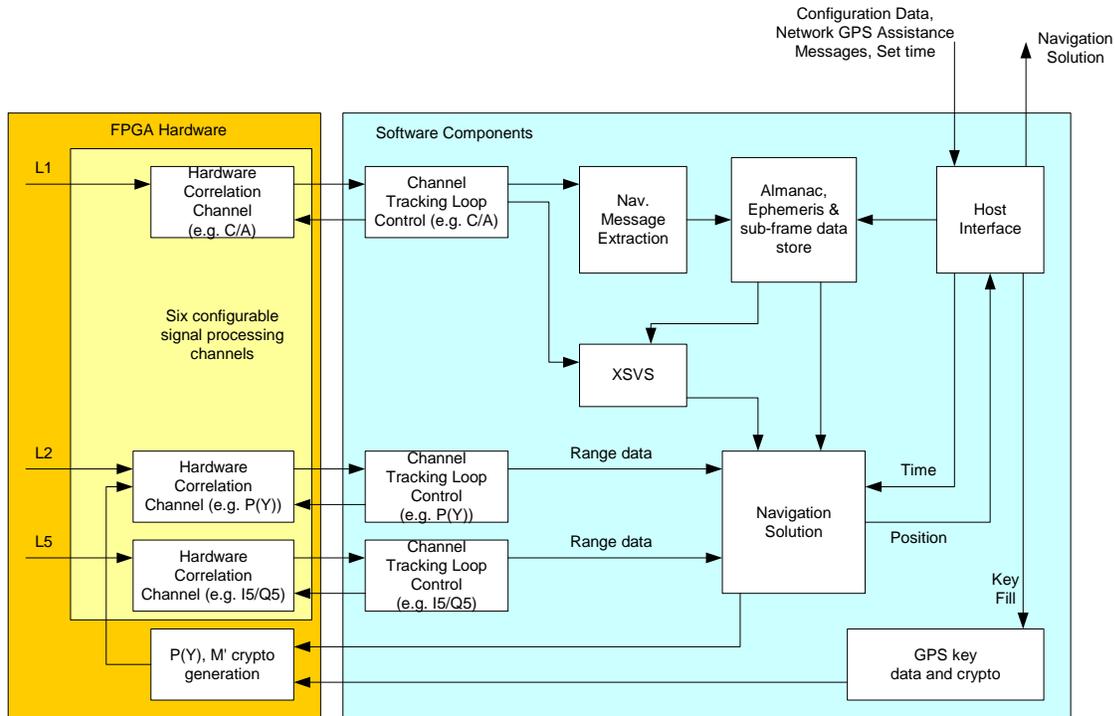
for any channel to be reconfigured in approximately 1.5 milliseconds.

## SOFTWARE AND FIRMWARE INTERACTION

All of the processors within the GNSS device are Xilinx MicroBlaze processors running code written in C/C++. Using the MicroBlaze approach allows a good tradeoff between dedicated hardware (the correlator channels) and software to implement each of the functions in the device. The tracking loops are implemented partially in hardware and partially in software. The software uses no operating system. It is implemented as a simple state machine which makes it easy to program and debug and ensures very well defined performance at runtime. The navigation processor is also a MicroBlaze running several tasks in a single state machine. The single navigation processor communicates with the tracking loop processors to set up and monitor the six tracking channels. The navigation processor also implements the interface to the host. Ephemeris data for the position, velocity and time (PVT) solution calculation can come from the navigation message extracted from the GPS signal channels (where available) or it can be provided by the host.

Figure 13 shows how the reconfigurable FPGA firmware and software components are used to track a set of GPS satellite signals. In this example, one channel is being used for C/A and two more are shown processing either P(Y) or the L5 I5 & Q5 signals. When at least one channel is used for C/A signal processing that channel can extract the GPS navigation data message sub-frames and generate the satellite almanac and ephemeris data. Each signal processing channel has an FPGA configuration that implements the correlation processing. The remainder of the

tracking loop is implemented in a software module. The software modules are also reconfigured based on the tracked signal type for each channel. The GNSS SDR design allows for any combination of the supported GPS signals to be implemented on each of the processing channels. The output of a single processing channel is a pseudorange measurement which is fed to the navigation solution computation component together with time and satellite ephemeris data. The computed position is available as an output from the GNSS SDR device to the host.



**Figure 13: Data Flow for Navigation Solution Computation**

**CONCLUSION**

Future GNSS receivers must be designed to deal with large numbers of GNSS available satellites and a wide variety of different GNSS code types. Over 90 satellites are projected to be launched by 2013 which will provide GNSS signals on many different frequencies and with dozens of different code types. By using dynamic reconfiguration of the GNSS receiver channels rather than a conventional fixed ASIC design approach, the channel resources can be reallocated to operate with any GNSS code/frequency pair to compute the optimum navigation solution from a subset of the many visible GNSS satellites. Only the receiver channels required are loaded and running on the FPGA at any given time. This allows for smaller devices to be used, consuming less power and having a smaller footprint than with fixed channel designs.

With the flexibility provided by a GNSS SDR, another advantage is that as new GNSS satellite signals or codes become available the SDR can be upgraded to handle these signals without deploying new hardware. Only the FPGA configuration file stored in flash memory would need to be changed. Upgrades could also be added to improve the GNSS receiver's performance including innovative algorithms to enhance the tracking performance in GPS-degraded environments, reduce multipath, or adapt to the presence of detected interference.

**ACKNOWLEDGEMENT**

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