PC/104 Test-Bed for Software GPS Receiver (SGR) and Software Defined Radio (SDR) Applications

Frank Carpenter, NAVSYS Corporation
14960 Woodcarver Road
Colorado Springs, CO 80921
(719) 481-4877 x137 (719) 481-4908 (fax)
e-mail: frankc@navsys.com

ABSTRACT

NAVSYS has developed a PC/104-based Software GPS Receiver (SGR) test-bed that integrates multiple sensors for advanced navigation applications. The sensors compatible with this system can provide GPS, wireless, inertial, and image information. This test-bed provides a low-cost hardware and software platform that can rapidly adapt to new waveforms and Software Defined Radio (SDR) applications.

PC/104-Plus systems are similar to standard desktop PCs but with a smaller embedded form factor of approximately 4" by 4" and with lower power consumption. PC/104-Plus boards typically use special stackable connectors carrying standard ISA and PCI bus signals. In addition, a PC/104-Plus system can use the same development tools and operating systems of full-sized PCs reducing the effort and cost of development.

The NAVSYS test-bed uses a commercial off-the-shelf PC/104-Plus processor card based on a Pentium-class, low-power processor. The processor card performs high-level processing and handles user interface and storage. In addition, it can interface to multiple sensors via the PCI bus or onboard serial ports.

We have developed a PC/104-Plus compatible Field Programmable Gate Array (FPGA) card with three low-cost, low-power Xilinx Spartan-3 chips to perform high-speed signal processing operations. The FPGAs can be used to perform correlation operations for GPS satellite tracking as well as other SDR signal processing. This FPGA card also contains high-speed sample buffer capability.

1. INTRODUCTION

Software Defined Radio (SDR) applications such as a Software GPS Receiver (SGR) require a flexible hardware architecture to support high performance processing for diverse range of RF transceivers and sensors. Preferably the hardware architecture is based on inexpensive, commercial off-the-shelf (COTS) components that use standardized interfaces.

NAVSYS has developed a test-bed based on the PC/104 standard. A COTS processor card is used to provide general purpose processing. We have developed a Field Programmable Gate Array (FPGA) card to perform high-speed signal processing algorithms. In addition, we have developed a simplified Digital Antenna Element (DAE) RF front-end. The test-bed was initially developed for GPS specific use, however it is being expanded to also allow academia to use components for SDR research.

2. PC/104 STANDARD

The PC/104 Consortium is a group of organizations formed in 1992 to standardize an open architecture for a small, embedded platform that is compatible with IBM personal computer systems. The initial PC/104 standard supported the ISA (Industry Standard Architecture) bus. However, it has evolved to the PC/104-Plus standard which now supports the PCI (Peripheral Component Interconnect) bus. In addition, there is a PCI only variant called PCI-104.

The PC/104 standards typically conform to a small size form factor of 3.6" x 3.8" as depicted in Figure 1. Two primary connectors are available on PC/104-Plus cards: a 104-pin, 16-bit ISA connector and a 209-pin, 32-bit PCI connector. Using these buses, PC/104 cards can interface and be mechanically stacked together. More information about these standards is available at the PC/104 consortium's website[1].

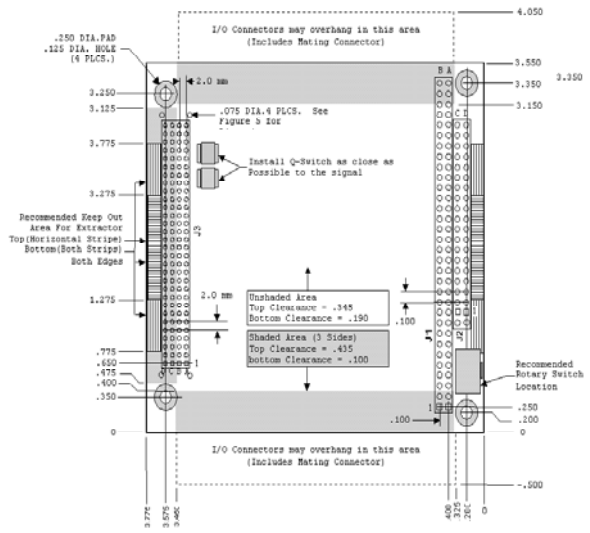

Figure 1 PC/104-Plus Form Factor

3. NAVSYS SGR/SDR TEST-BED

Figure 2 shows the high-level core architecture of the NAVSYS SGR/SDR. Multiple Digital Antenna Elements RF front-ends are used to convert between analog radio signals and digital signals. An FPGA card provides high speed signal processing. A General Purpose Processor (GPP) provides higher level processing and user or application interface control. In some applications, a security processor is used for crypto functions. We have used this same architecture previously on PC and CompactPCI platforms[2,3,4]. We are now using it on PC/104 platforms

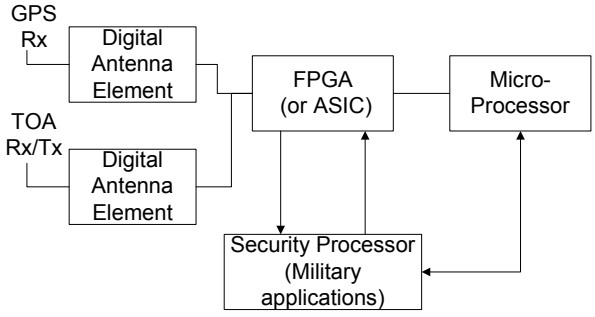

Figure 2 SGR/SDR Architecture

NAVSYS has been developing integrated navigation applications using network assistance and time-of-arrival (TOA) capabilities. Figure 3 shows a PC/104-based test-bed that we are using to research these features. The PC/104 stack contains the FPGA and Microprocessor resources. An L-Band (1575.42MHz) GPS DAE and 900MHz DAE are added for GPS and TOA. In addition, a standard 802.11 wireless network connection is used to provide network assistance and data sharing.

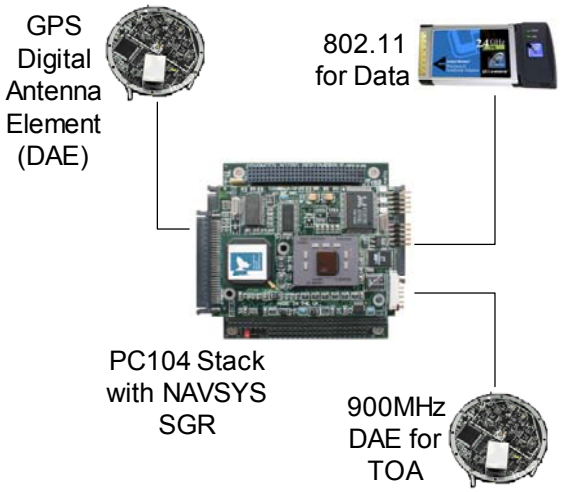

Figure 3 NAVSYS PC/104 SGR/SDR Test-Bed

We are using this SGR/SDR test-bed to develop the software and firmware to track the GPS signals in the SGR and also to provide a TOA signal using the 900 MHz DAE for use as a back-up navigation mode. This signal provides TOA aiding by phase locking the broadcast 900 MHz signal to GPS time derived from tracking the GPS time reference signal. The TOA spread-spectrum signal used allows multi-channel access and also provides excellent interference rejection properties to other transmitters operating in the ISM band. The data link uses simplex or half-duplex data transmission to allow full use of the 902-928 MHz spectrum for the spread spectrum transmission. Different TOA transmitting channels are identified by the PRN code that they select for the encoding.

Network assistance is used to bolster GPS reception in low signal and degraded signal environments (e.g., tunnels, buildings, under tree canopy, and within proximity to RF transmissions). TOA positioning assistance is also used for areas where GPS reception is impossible using strategically located test-bed nodes.

4. PC/104-PLUS PROCESSOR CARD

We have evaluated several PC/104 vendors and have selected two different processor cards for our SGR applications. One is based on the Crusoe TM5x00 processor. The other is based on the Pentium-M processor. The primary difference between the two boards is performance and power. The PC/104-Plus

processor card stack is shown below in Figure 4, and has the following specifications:

- 100% PC-AT compatible
- Crusoe TM5x00 processors to 667MHz or Pentium-M processors to 1.6GHz
- 64 - 1024MBytes SDRAM
- 10/100MBit Ethernet
- EIDE and USB ports
- Low Power ACPI compliant
- PC/104-Plus and PC/104 Expansion
- Available in Extended Temperature
- Standard 3.6in x 3.8in PC/104 form factor
- Total stack power consumption is 10-30W depending on hardware configuration, processor and application

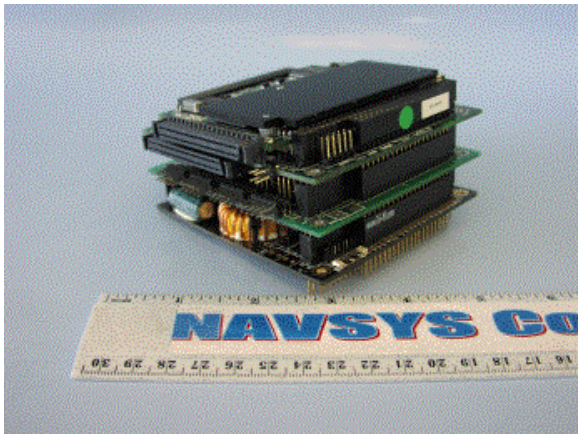

Figure 4 PC/104-Plus SGR/SDR PC/104 Stack

The processor card can support multiple operating systems. NAVSYS is using two different operating systems for SGR development on the PC/104-Plus test-bed: Windows XP and Linux. Most of our work involves applications that require real-time deterministic performance. In order to more easily support real-time data transfer with direct memory access (DMA), we are using real-time kernel enhancements to these operating systems. For Windows XP, we are using RTX (real-time extensions for Windows) from VenturCom. For Linux, we are using RTLinuxPro from FSM Labs. Both provide sub-10µs interrupt latencies. For soft real-time application, any operating system that can run on a Pentium-class standard PC can also run on the PC/104-Plus processor card.

5. DIGITAL ANTENNA ELEMENT (DAE)

The DAE provides some useful features for SGR and SDR applications:

- Small size; approximately 3" diameter/square.
- Low power consumption.
- Simplified RF interface. Abstracts analog domain from processing components.
- Currently uses LVDS (low-voltage differential signaling) over standard category-5 twisted pair cable. USB and IEEE 1394 Firewire available for future DAEs.
- LVDS interface provides ability to develop diverse range of antenna elements for different bandwidths/frequencies with a common interface to FPGA card.
- Sampling rate controllable via far end. Clock can be provided through LVDS pairs for phase-coherent operation, and reduces noise and power introduced by an on-board oscillator.
- Converts analog RF signal to digital domain close to antenna. Minimize cable interference.
- Supports active or passive antenna arrangements. SMA connector available.

The GPS DAE, depicted in Figure 5, down-converts and samples GPS RF signals and provides a serial digital output to the SGR FPGA card which performs the GPS code generation and correlation. It is capable of receiving both L1 and L2 GPS signals.

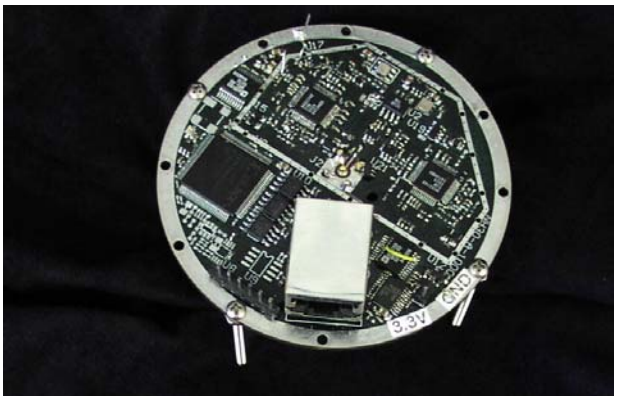

Figure 5 GPS Digital Antenna Element

We have also developed a 900MHz transceiver DAE that performs the functions of receiving, down-converting and sampling the received data link signals and modulating and transmitting the broadcast signals. The received digitized signals are passed to the processing firmware and software where the signals are demodulated. The transmitted digital signals are similarly generated using the firmware and software and up-linked to the 900MHz DAE for modulation on the RF broadcast. Both the GPS DAE and the 900MHz DAE are designed to operate from a common sample clock and phase-

locked reference LO. This requirement assures that the timing between the two signal sources is precisely phase locked. The design will accommodate different frequencies for the transceiver.

900MHz DAE Design Specs:
RF Frequency Range: 902 ~ 928MHz
Bandwidth: 26MHz
Analog IF Center Frequency: 15MHz
Sampling Rate: 56MHz for 26MHz bandwidth
(40MHz for 20MHz BW or less)
Bits per Sample: 14
SFDR: 86dBc

L-Band GPS DAE Design Specs:
RF Frequency Range: L1 (1575.42MHz)
and L2 (1227MHz)
Bandwidth: 20MHz
Analog IF Center Frequency:
15.42MHz for L1, 18.6MHz for L2
Sampling Rate: 40MHz
Bits per Sample: 8

6. PC/104 FPGA Card

NAVSYS had developed a PC/104-Plus FPGA card as depicted in Figure 6. This card contains three Xilinx Spartan-3 FPGAs used to perform high-speed correlations and firmware-based signal processing. Bit-files loaded on the FPGAs are developed using VHDL. LVDS connections can be used for the GPS DAE or other DAEs.

Figure 6 PC/104-Plus FPGA Card

The FPGA card also contains a PCI bus chip to provide high speed interfacing between the FPGAs and the processor card over the PC/104-Plus PCI bus. The PCI bus chip also provides interrupt and DMA capabilities. We have measured a sustained data rate of 72 megabytes per second with our current FPGA card using DMA data transfer (the theoretical maximum bandwidth is 33 MHz by 32 bits or 133 Mbytes/sec).

The FPGA card also contains an SRAM buffer for storing samples. This sample buffer can be DMAed to the host processor for analysis. We have used this buffer for FFT-based satellite acquisition.

7. OTHER SENSORS

Because of the flexibility of the PC/104 architecture, the SGR/SDR test-bed can support a wide array of interfaces and sensors. We are using interfaces such as RS-232, USB, and IEEE 1394 Firewire to a variety of navigation and communication sensors. Some sensors that we have used include accelerometer, gyroscope, Inertial Measurement Unit (IMU), barometer/altimeter, and a camera. Figure 7 and Figure 8 show sensors that we are using with the test-bed. Figure 9 shows a block diagram of an application using many of these sensors.

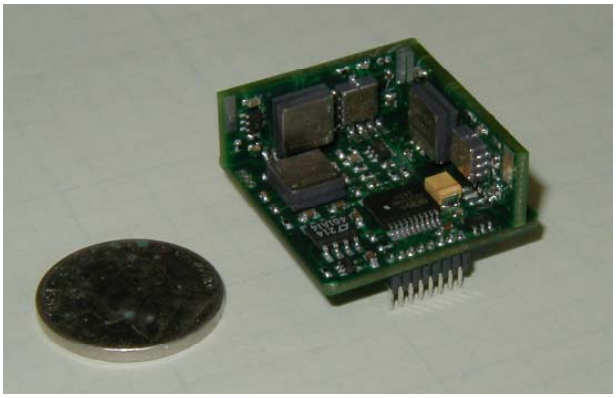

Figure 7 Small MEMS Inertial Measurement Unit (1"x1"x 0.5")

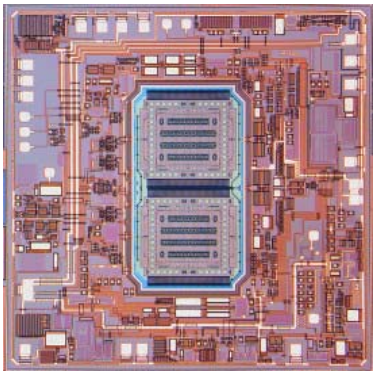

Figure 8 Analog Devices ADXRS150 Gyro

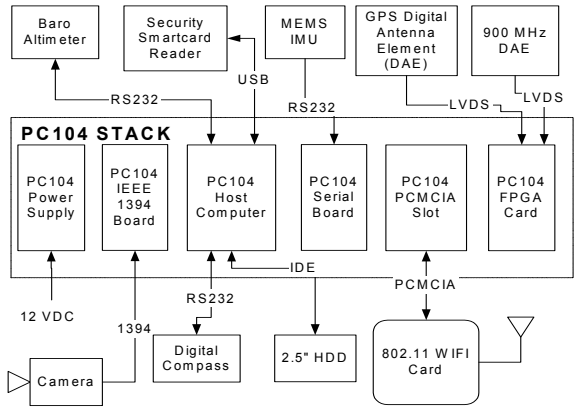

Figure 9 PC/104-Plus SGR Test-bed Application

8. FUTURE

The SGR/SDR PC/104 test-bed is being used as a development platform for next generation positioning and communications applications including transitioning into the Joint Tactical Radio System (JTRS). In the future, we plan to support development of the Virginia Tech open-source C++ SCA implementation with an embedded target (OSSIE) of the NAVSYS PC-104 test-bed. This would include development of a SCA-compliant device wrapper for the NAVSYS SGR and a 900 MHz SDR data link. This will be used to support a demonstration of the integrated SDR/SGR positioning and communications functions.

This system will also serve as an inexpensive reference platform for universities and industries interested in developing SCA-based waveforms.

JTRS development is currently hampered by expensive cost to entry with existing solutions. By encouraging the proliferation of JTRS and SCA development on a relatively low-cost hardware/software platform, this can enable more rapid introduction of new waveforms and software radio applications. Currently, the JTRS development system used to develop SCA compliant waveforms are cost prohibitive for most universities.

Although the OSSIE test-bed would not include all of the functionality of commercial, full development, it can provide a low cost, open-source, development platform for SCA-based waveforms suitable for use by industry and academia.

There has also been significant interest in using the PC/104 FPGA card and DAEs with a standard PC platform. A PC/104-Plus-to-PCI adapter can be used to interface the FGPA card to a standard PC PCI bus.

9. CONCLUSION

Some of the advantages of Software GPS Receiver/Software Defined Radio PC/104 test-bed are summarized below.

Multi-Frequency, Multi-Mode Operation.
The nature of the PC/104 test-bed and SDR approach simplifies the introduction of additional frequency channels and the tracking of new codes. New frequencies are supported by developing a simple Digital Antenna Element RF front end that complies with the PC/104 FPGA board and DAE LVDS interface standard.

Flexibility and Upgradeability.
The reprogrammable nature of the software defined radio allows it to be upgraded through firmware and software modifications. This provides a forward upgrade path for adding new waveforms.

Standard Hardware and Interfaces.
The SGR/SDR test-bed uses PC/104 and other PC industry standardized interfaces. By adding additional PC/104 cards as well as RS-232, USB and IEEE 1394 Firewire components one can easily expand the system.

Robust, Inexpensive Development Tool.
This test-bed is relatively inexpensive platform for SGR and SDR applications. The system builds upon proven PC processor and chipset technology reducing development time and effort.

10. ACKNOWLEDGEMENTS

NAVSYS gratefully acknowledges support of the US Army and CECOM (Communications - Electronics Command) for sponsoring efforts to develop the PC/104-Plus SGR Test-bed.

11. REFERENCES

1 PC/104 Consortium Website (http://www.pc104.org/)
2 K. Gold and A. Brown, "A Software GPS Receiver Application for Embedding in Software Definable Radios," Proceedings of ION GPS 2003, Portland, Oregon, September 2003
3 A. Brown, K. Gold, and M. Nylund, "A GPS Software Application for Embedding in Software Definable Radios," Proceedings of 13th Virginia Tech Symposium on Wireless Personal Communications, Blacksburg, VA, June 2003.
4 N. Gerein and A. Brown, "Modular GPS Software Radio Architecture," Proceedings of ION GPS 2001, Salt Lake City, UT, September 2001